

SHEET

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PH7 PH8 PH1 PH2 PH9 PH10 PH3

PH4

PH11

PH12

PH5

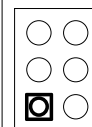
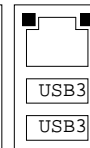
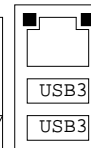
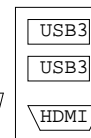
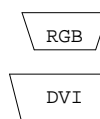
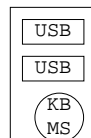
PH6

CPU SOCKET

2 oz PCB

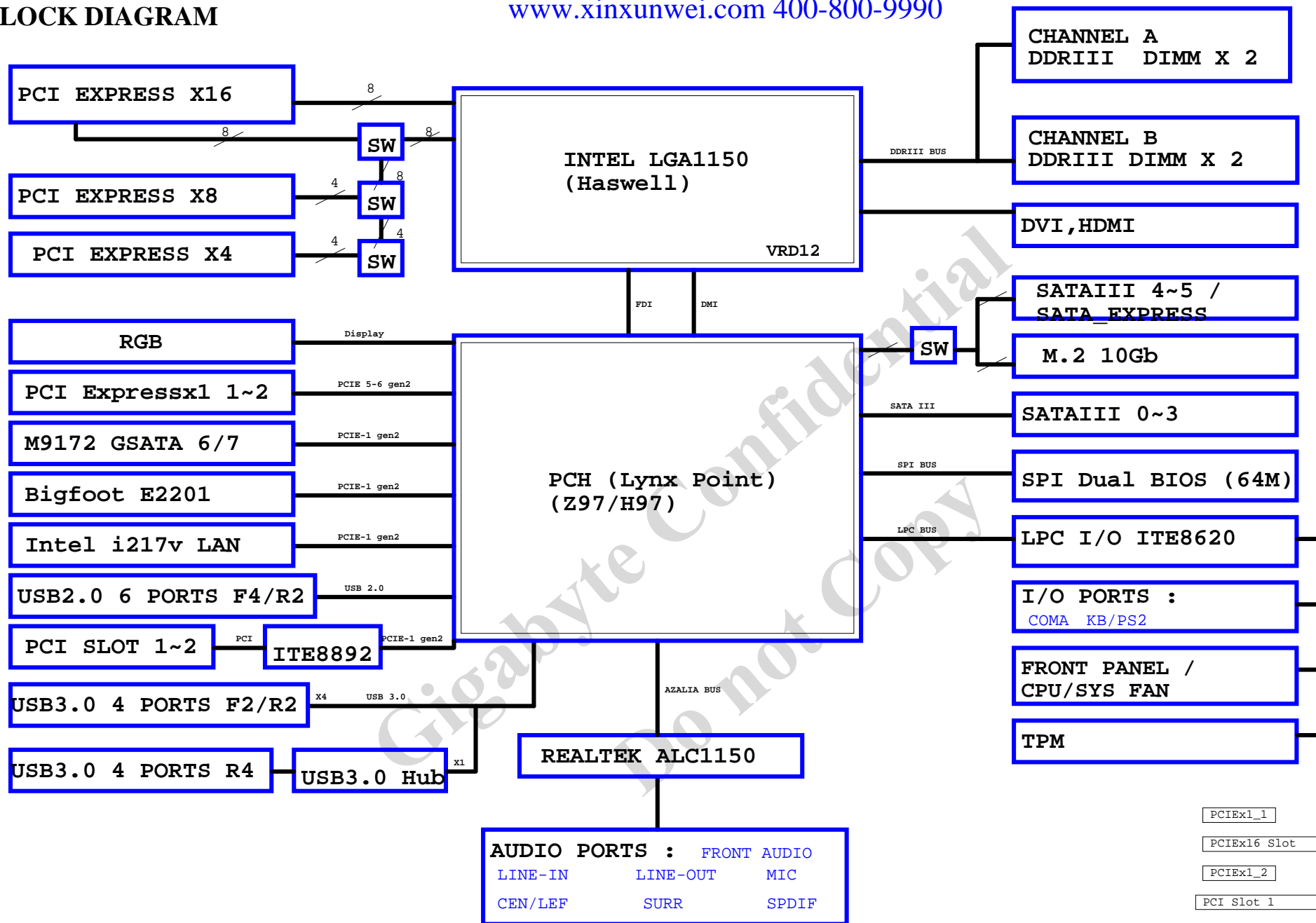
Gigabyte Technology

Title			Cover Sheet		
Size	Document Number	GA-Z97X-UD5H			Rev
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BLOCK DIAGRAM

www.xinxunwei.com 400-800-9990



PCIEx1_1

PCIEx16 Slot

PCIEx1_2

PCI Slot 1

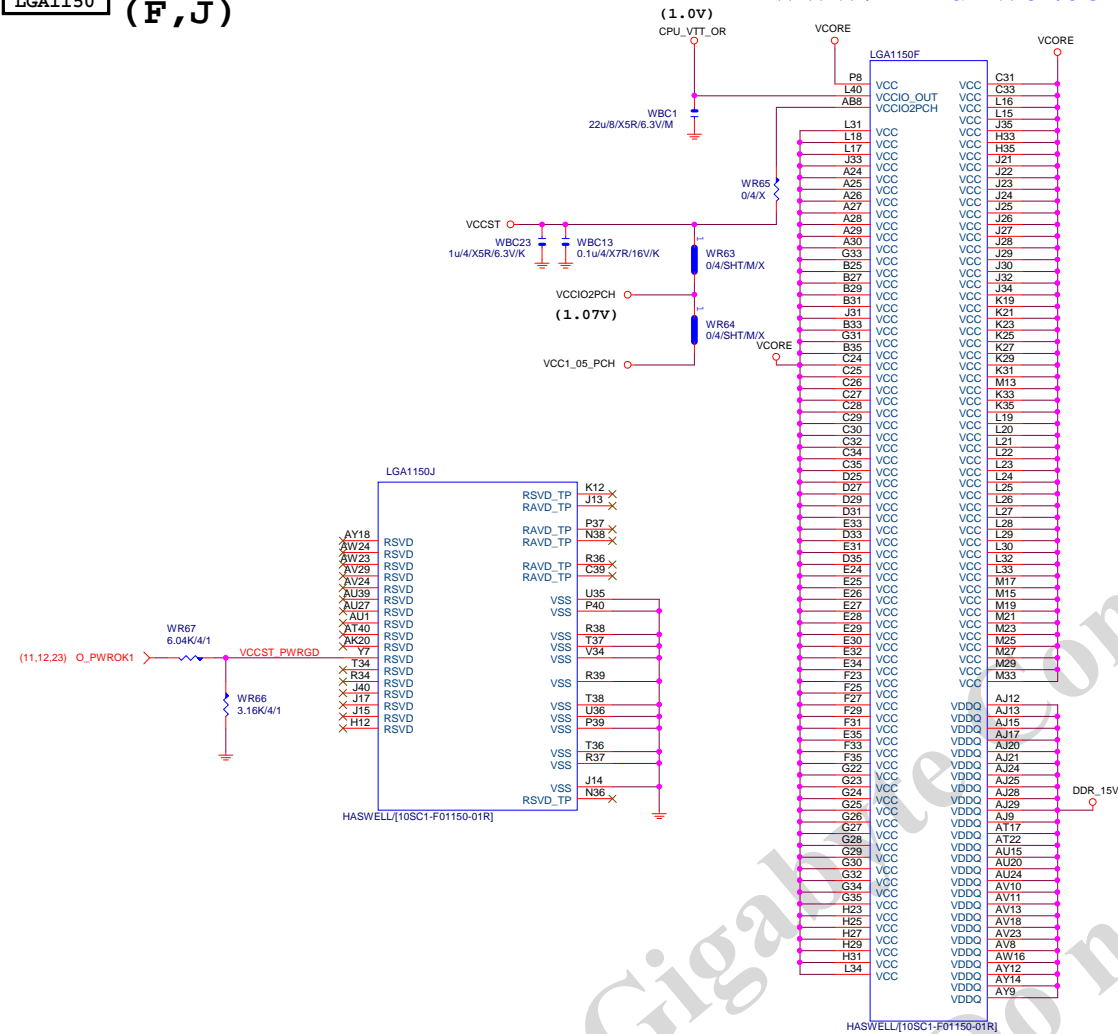
PCIEx8

PCI Slot 2

PCIEx4

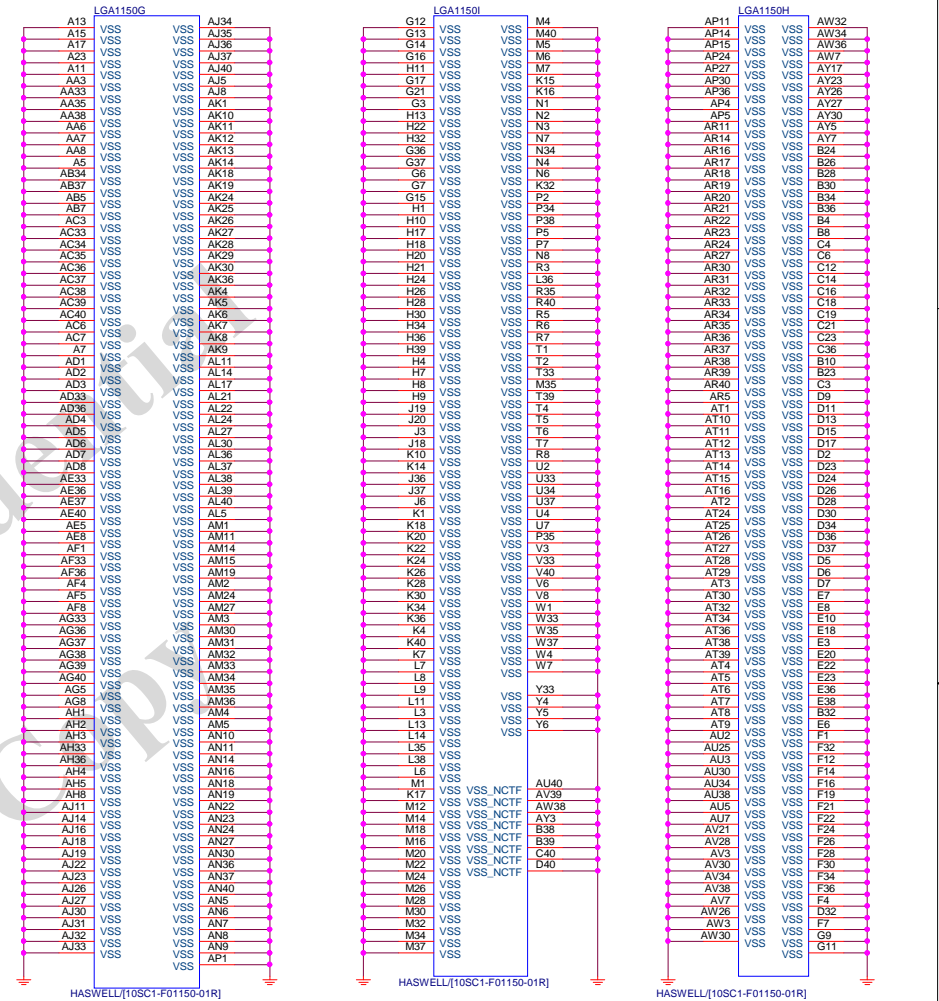
LGA1150

(F, J)



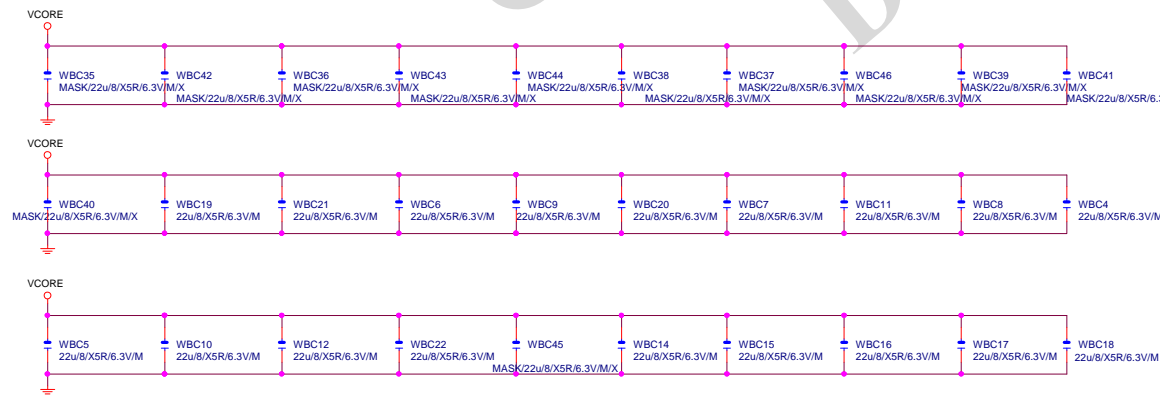
LGA1150

(G, H, I)



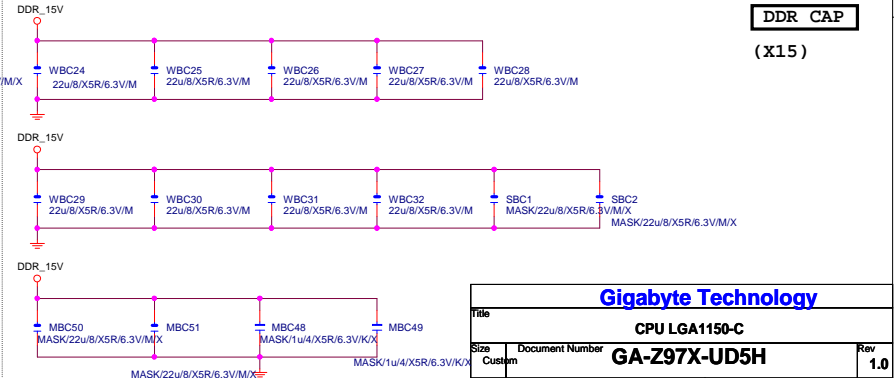
VCore CAP

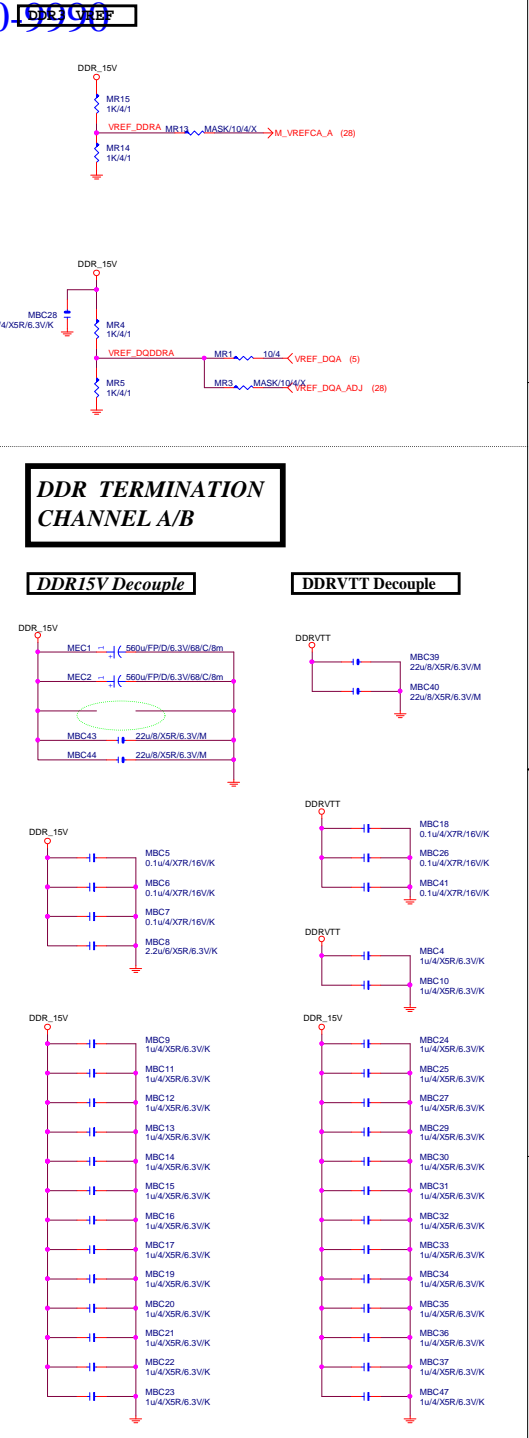
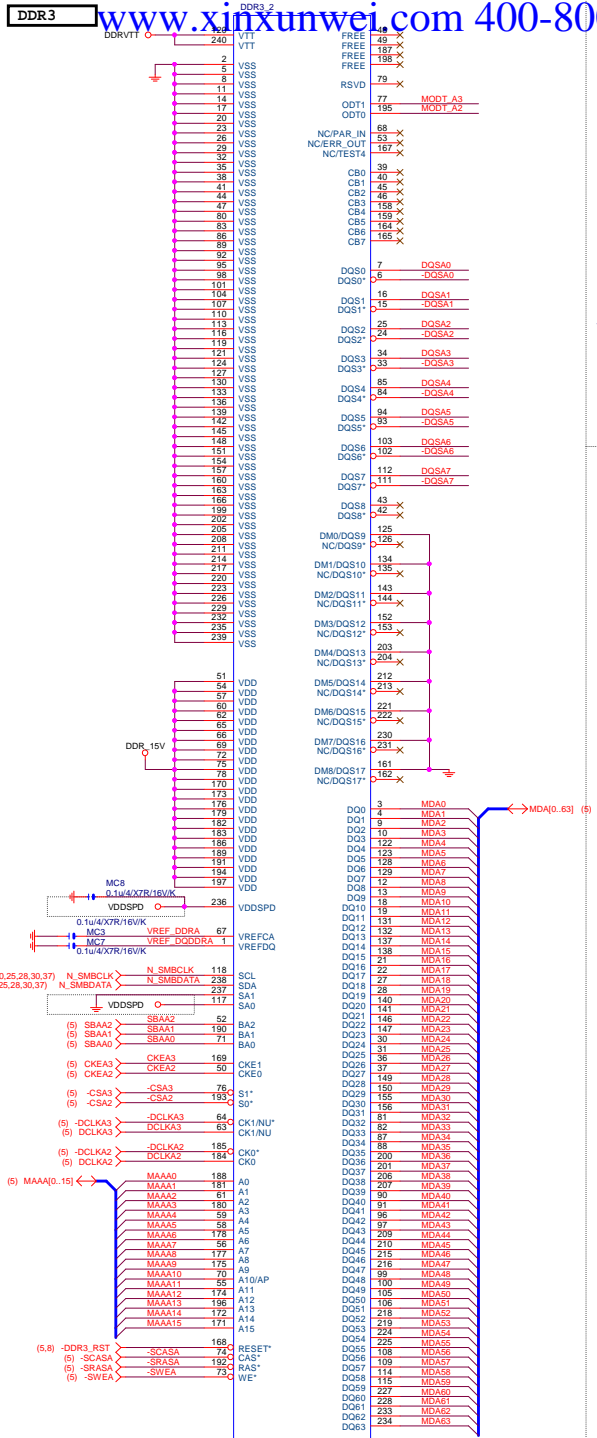
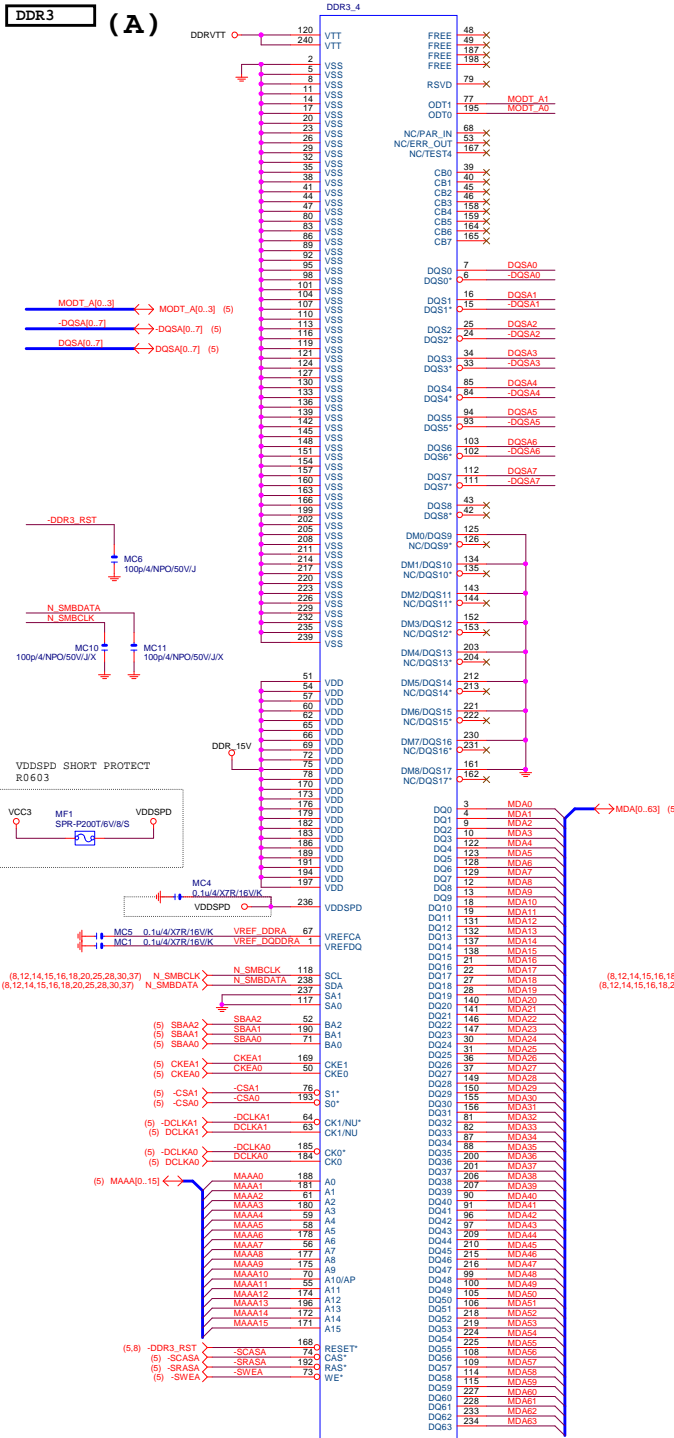
(X30)



DDR_15V

(X15)

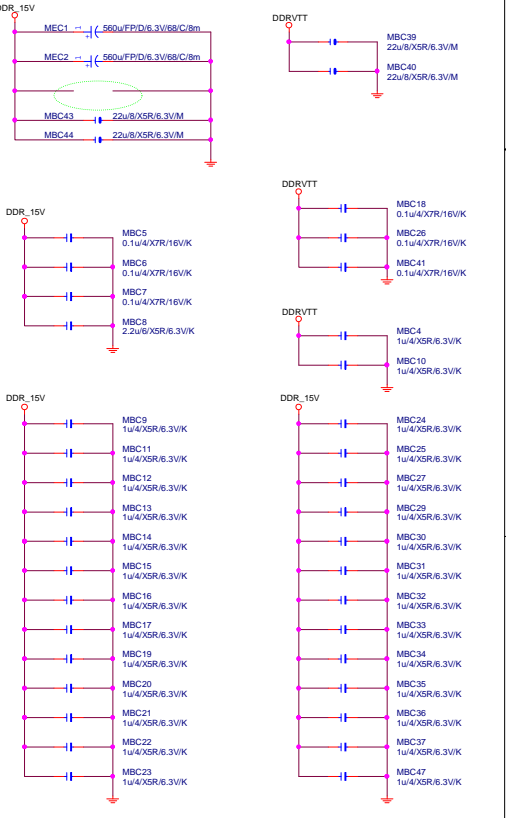


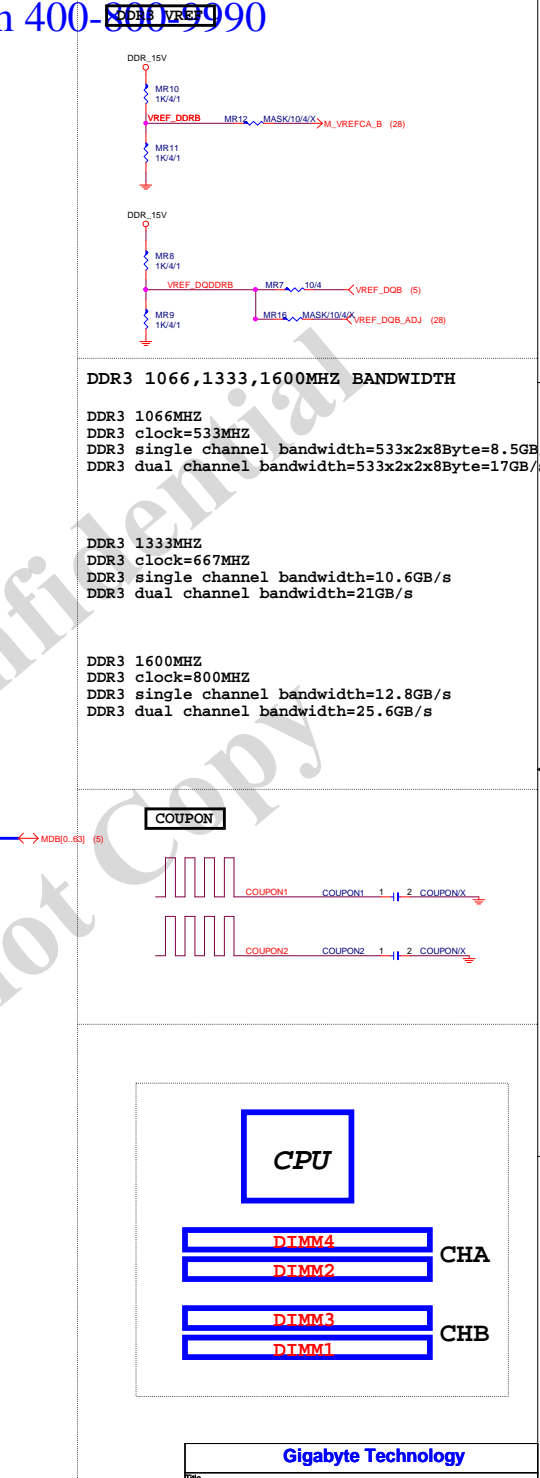
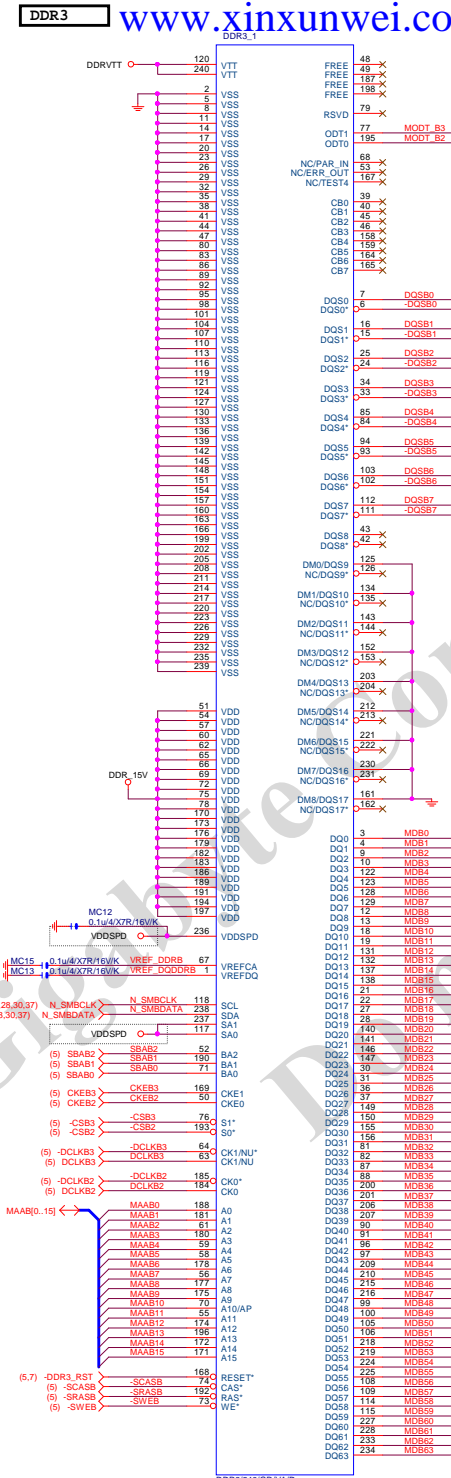
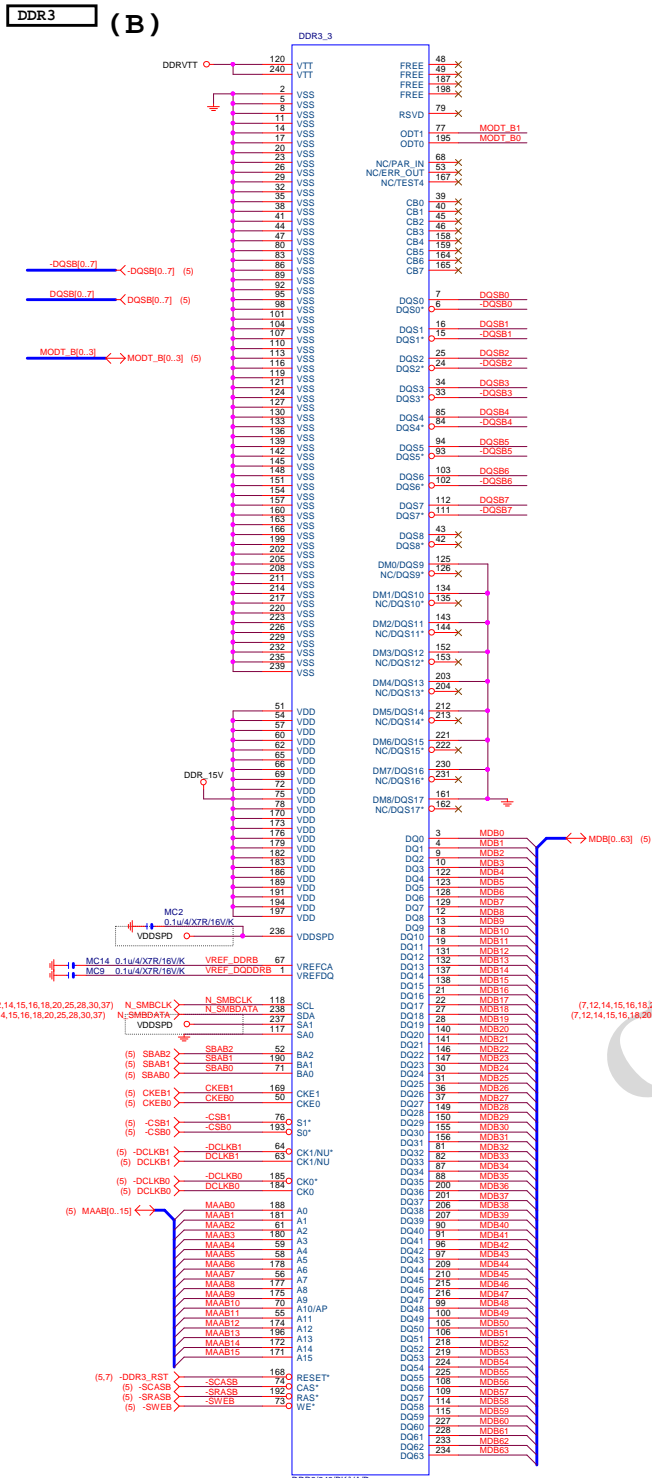


DDR TERMINATION CHANNEL A/B

DDR15V Decouple

DDRVTT Decouple





PCH (B)

DMI:12/4/4/12(breakout min 8/4/4/4/8)
Impedance=85 +- 17.5%

USB2.0 : 12/5/7/5/12 (breakout min 8/4/4/4/8)
Impedance=85 +- 15%

(4) A_DMI_0TXN A_DMI_0TXP L24
(4) A_DMI_0RXN A_DMI_0RXN K24
(4) A_DMI_0RXP A_DMI_0RXP B20
(4) A_DMI_1TXN A_DMI_1TXN C24
(4) A_DMI_1TXP A_DMI_1TXP H24
(4) A_DMI_1RXN A_DMI_1RXN D21
(4) A_DMI_1RXP A_DMI_1RXP B21
(4) A_DMI_2TXN A_DMI_2TXN F26
(4) A_DMI_2TXP A_DMI_2TXP G26
(4) A_DMI_2RXN A_DMI_2RXN B26
(4) A_DMI_2RXP A_DMI_2RXP C22
(4) A_DMI_3TXN A_DMI_3TXN K26
(4) A_DMI_3TXP A_DMI_3TXP L26
(4) A_DMI_3RXN A_DMI_3RXN A24
(4) A_DMI_3RXP A_DMI_3RXP B24

PCB H
DMI_RXN_0
DMI_RXP_0
DMI_TXN_0
DMI_TXP_0
DMI_RXN_1
DMI_RXP_1
DMI_TXN_1
DMI_TXP_1
DMI_RXN_2
DMI_RXP_2
DMI_TXN_2
DMI_TXP_2
DMI_RXN_3
DMI_RXP_3
DMI_TXN_3
DMI_TXP_3
DMI_RCOMP
PCI_E_RCOMP
CLKIN_DMI_N
CLKIN_DMI_P

VCC1_5_PCH
W=8 mil out of PCH
S=15 mil to other signals

USB 3. Hub
B85/H81:USB N/A

LAN E2201

ITE8892 PCI
Bridge

PCIEX1_1

PCIEX1_2

Marvell 9172

H81:PCIE 7/8X
I217V LAN

電容放靠近 Device & PCI-E Slot

Z97/S[10HB1-030Z97-20R]

PCB PCIE ,DMI 4/4/4//15 Impedance=85 +- 15%

usb2.0 5/7/5//12

usb3.0 5/7/5//20

N_-USBOC_F
NBC82
0.1u4/X7R/16V/K

N_-USBOC_R
NBC83
0.1u4/X7R/16V/K

PCH (F)

Port要對應

B85/H81: 5/7 N/A

H81:12/13 N/A

H81:USB3.0 N/A

(30) PCH_USB3_RXN0
(30) PCH_USB3_RXP0
(30) PCH_USB3_TXN0
(30) PCH_USB3_TXP0
(30) PCH_USB3_RXN1
(30) PCH_USB3_RXP1
(30) PCH_USB3_TXN1
(30) PCH_USB3_TXP1
(34) PCH_USB3_RXN4
(34) PCH_USB3_RXP4
(34) PCH_USB3_TXN4
(34) PCH_USB3_TXP4
(34) PCH_USB3_RXN5
(34) PCH_USB3_RXP5
(34) PCH_USB3_TXN5
(34) PCH_USB3_TXP5

PCBF

USB3
FDILINK
N1 FDI_TXN0
N2 FDI_TXP0
P2 FDI_TXN1
P3 FDI_TXP1
L2 FDI_CSXNC
L3 FDI_INT
K2 NR29 7.5K/4/1 VCC1_5_PCH
FDI:12/4/5/4/12
Impedance=85 +- 17.5%

FDI_TXP[0..1] FDI_TXN[0..1]
FDI_TXP[0..1] FDI_TXN[0..1]

USB3.0:20/5/7/5/20 (breakout min 8/4/4/4/8) ; ONLY 3 VIAS
Impedance=85 +- 17.5%
Back Panel < 10000 MILS
Front Panel < 6000 MILS

Mount for integrated clock Generation Mode

CK_SRCLK_PCH NR89 8.2K/4
CK_SRCLK_PCH NR88 8.2K/4
CK_DOTCLK NR92 8.2K/4
CK_DOTCLK NR91 8.2K/4
NR92 short to GND in non graphic SKU

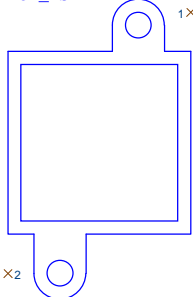
PCH (J)

PCB H

AT1 VSS_NCTF TP22 U11
AT1 VSS_NCTF TP23 U10
AV1 VSS_NCTF TP21 AK14
AV2 VSS_NCTF TP20 K34
AV40 VSS_NCTF TP14 K33
AV41 VSS_NCTF TP15 AH24
AW2 VSS_NCTF TP10 L16
AW40 VSS_NCTF TP11 K16
B40 VSS_NCTF TP9 AM34
B41 VSS_NCTF TP3 R12
C41 VSS_NCTF TP4 N12
D1 VSS_NCTF TP1 L22
D41 VSS_NCTF TP2 K22
R4 R5
TP6 K5
TP7 P5
TP8 L5
AC31
VSS AF3
VSS AV21

PCB H/S

PCB_HS



PCB_HS[12SP2-PTZ975-01R_12SP2-PTZ975-02R_12SP2-PTZ975-03R]

MOS heatsink + PCH heatsink

USB TABLE

OC[3:0]# for Device 29 (ports 0-7)

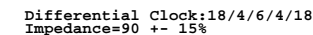
OC[7:4]# for Device 26 (ports 8-13)

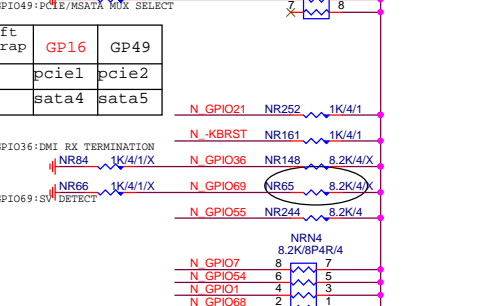
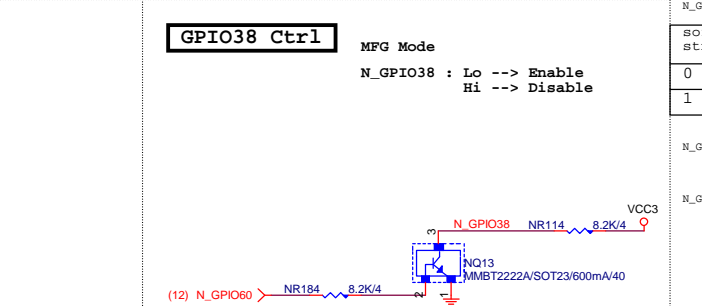
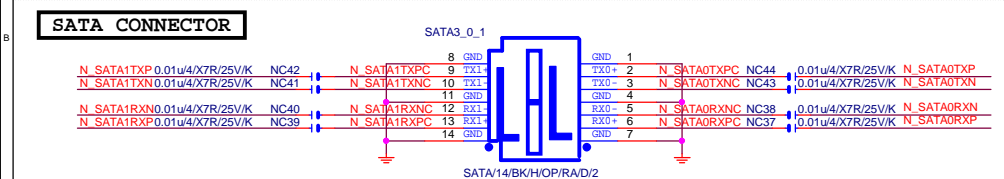
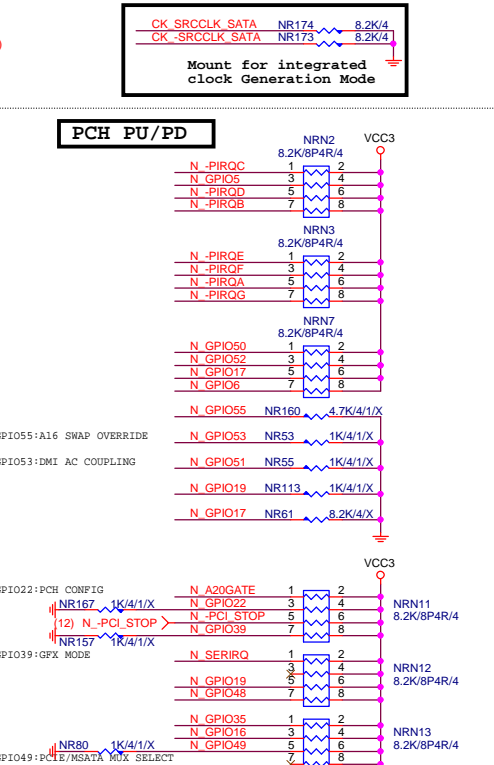
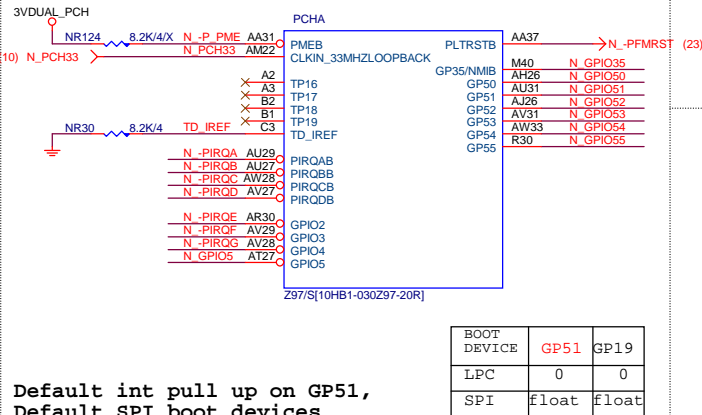
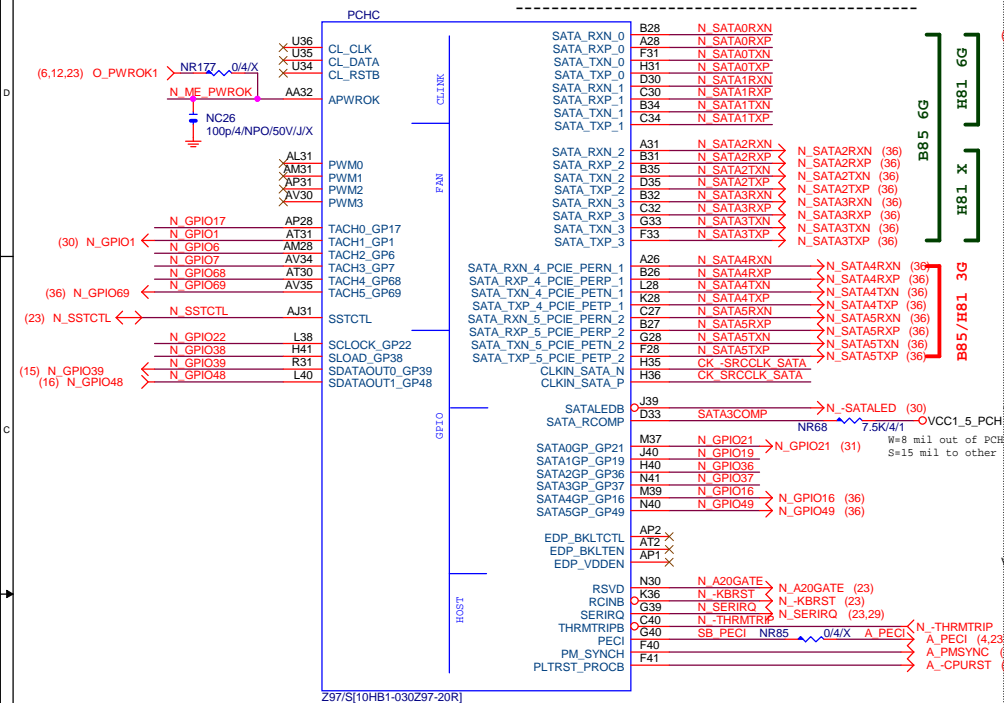
USB Usage & OC# Configure

OC0#	USB0,1	F_USB30	FUSEVCC_F1_F2
OC1#	USB2	USB3_LAN1	UC_FUSEVCC34
	(U3 Hub)	USB3_LAN2	UC_FUSEVCC12
OC2#	USB4,5	HDMI & R_USB3	FUSEVCC_R1_R2
	USB6,7	N/A	
OC4#	USB8,9	KB_MS_USB	FUSEVCC_R3_R4
OC5#	USB10,11	F_USB2	FUSEVCC_F5_F6
OC6#	USB12,13	F_USB1	FUSEVCC_F3_F4
OC7#	Not Use		

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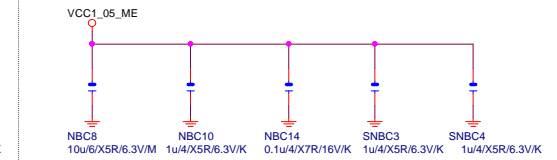
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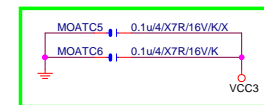
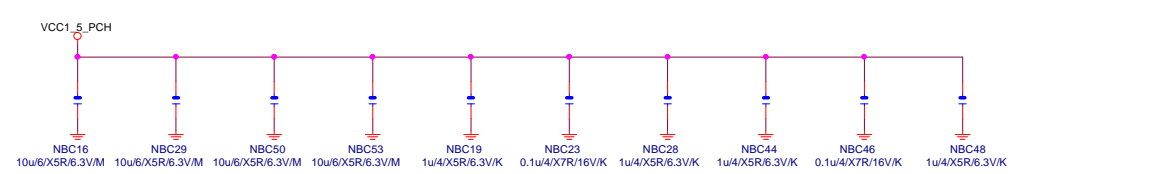
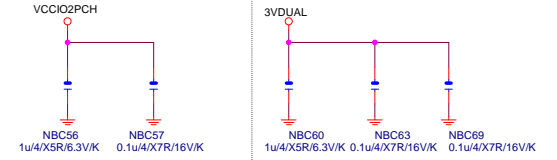




(1.05V) (x5)



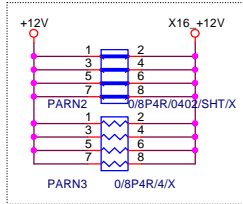
(1.05V)(X2) (3.3V) (X3)



**+12 protect
short-wire test**

PCIE16:16/5/5/16

PA_EXP_RXP0[.15] >> PA_EXP_RXP0[.15] (4,17)
PA_EXP_RXN0[.15] >> PA_EXP_RXN0[.15] (4,17)
PA_EXP_TXP0[.15] >> PA_EXP_TXP0[.15] (4,17)
PA_EXP_TXN0[.15] >> PA_EXP_TXN0[.15] (4,17)



PA_EXP_SW_RXP8[.15] >> PA_EXP_SW_RXP8[.15] (17)
PA_EXP_SW_RXN8[.15] >> PA_EXP_SW_RXN8[.15] (17)
PA_EXP_SW_TXP8[.15] >> PA_EXP_SW_TXP8[.15] (17)
PA_EXP_SW_TXN8[.15] >> PA_EXP_SW_TXN8[.15] (17)

PCI-E REV:1.1--> 2.5GHZ

PCE-E X1(單向) BANDWIDTH=2.5GHz*(8b/10b)=2Gb/s=250MB/s

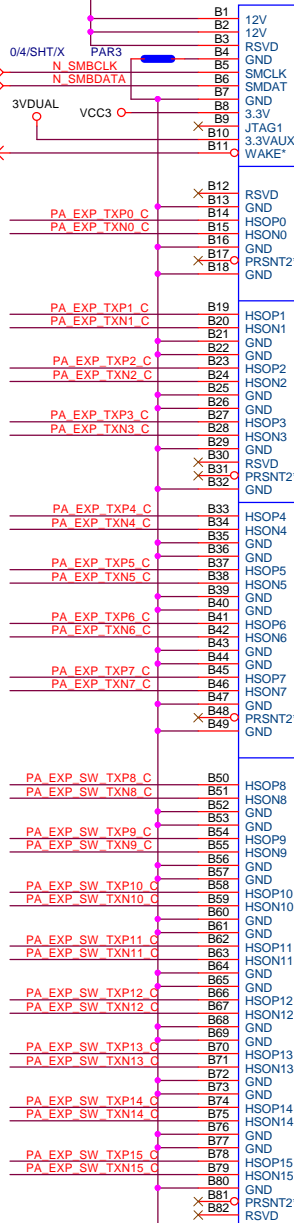
PCE-E X1(雙向) BANDWIDTH=2.5GHz*(8b/10b)X2=4Gb/s=500MB/s

PCE-E X16(單向) BANDWIDTH=2.5GHz*(8b/10b)X16=32Gb/s=4GB/s

PCE-E X16(雙向) BANDWIDTH=2.5GHz*(8b/10b)X16X2=64Gb/s=8GB/s

PCI-E REV:2.0--> 5GHZ

PCIE16:16/5/5/16

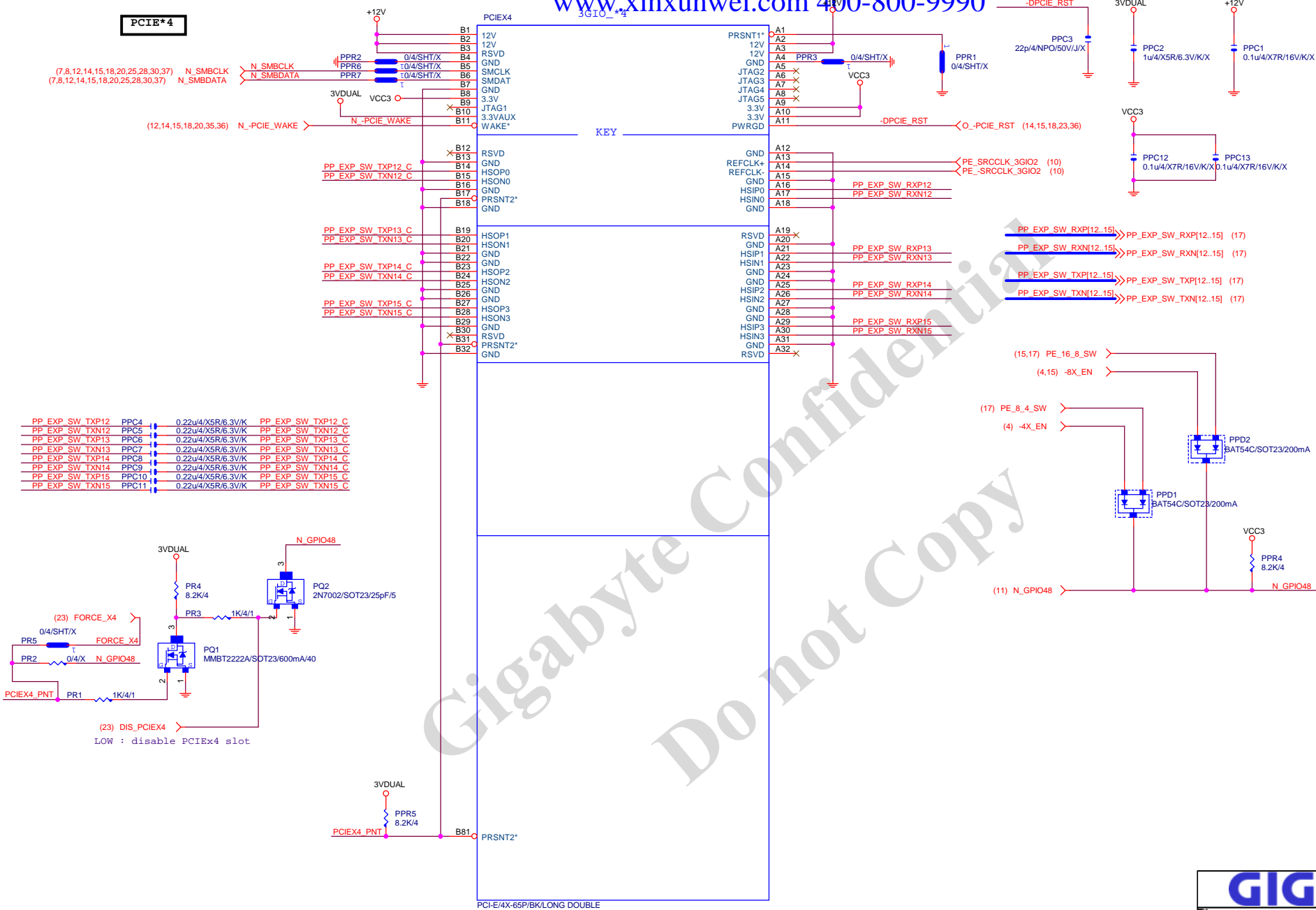


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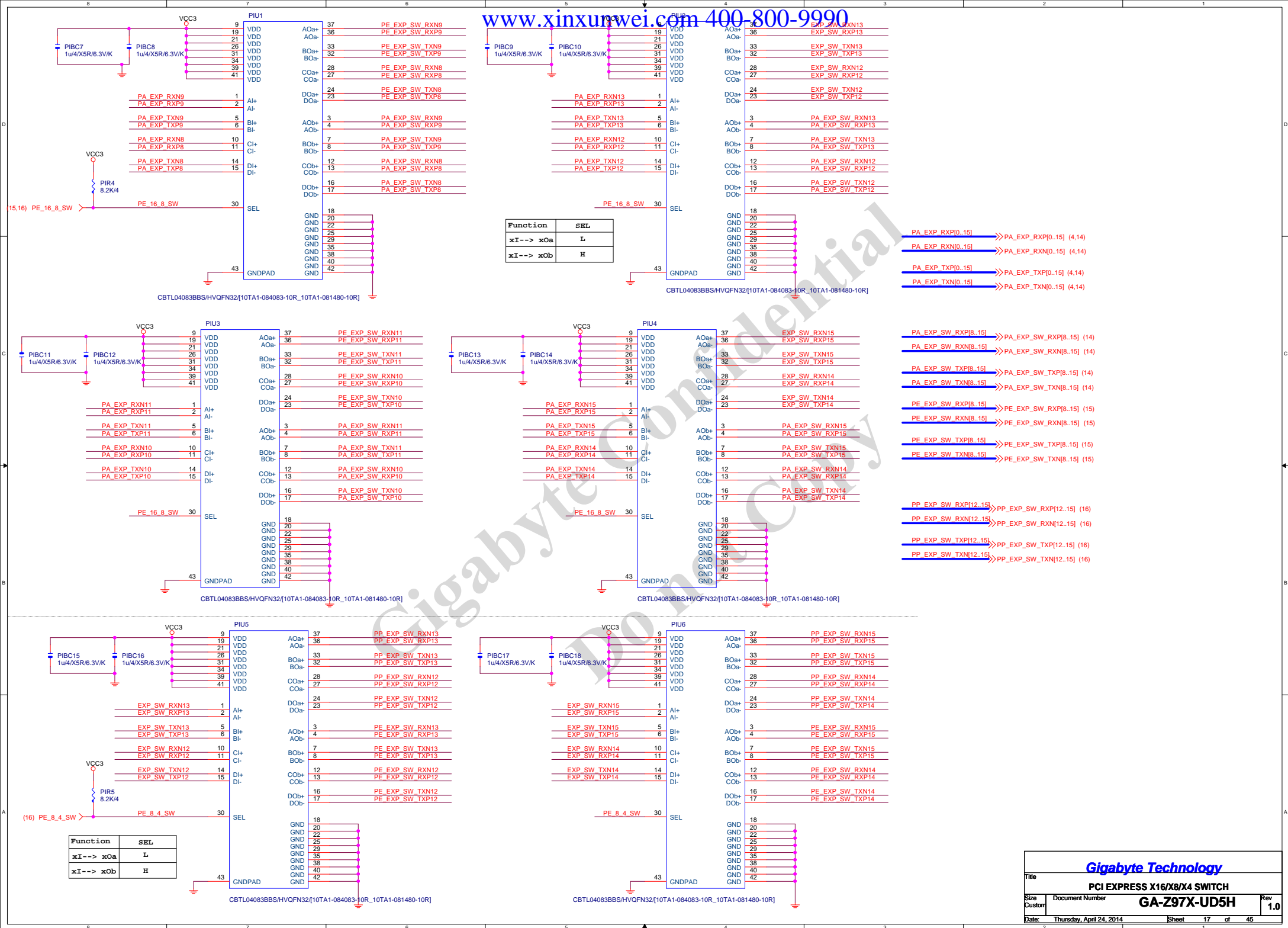
Gigabyte Technology

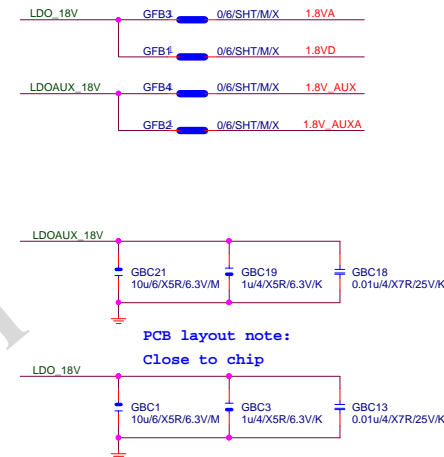
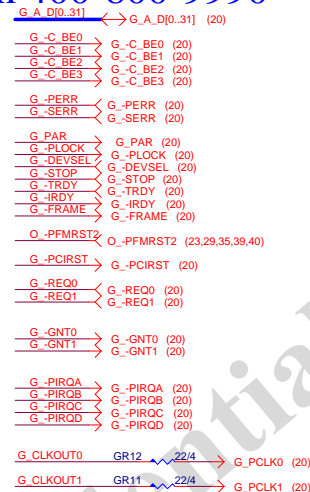
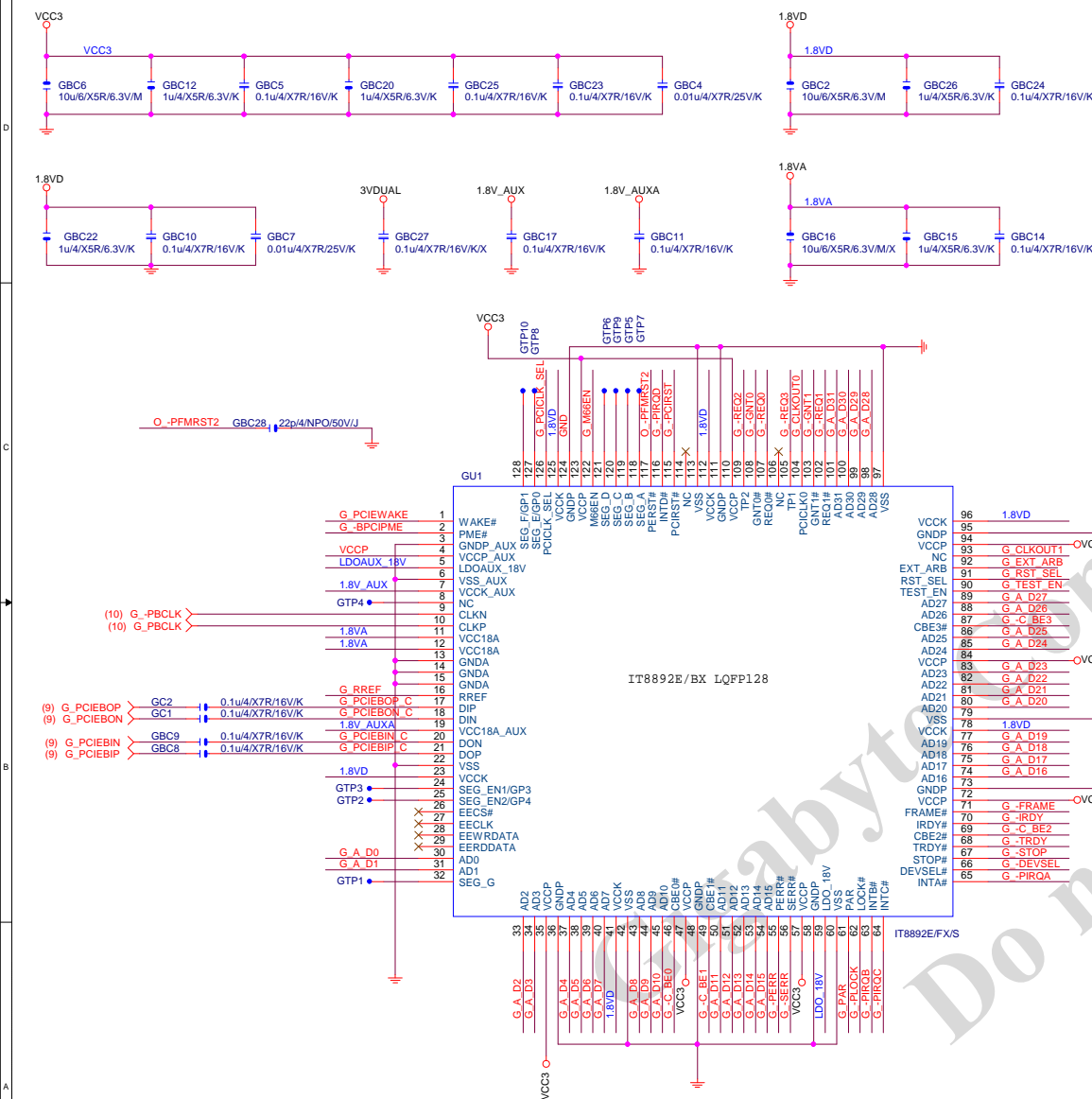
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PCIE*4

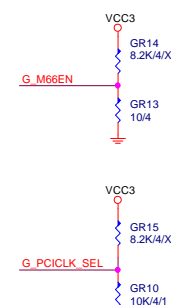
**GIGABYTE™**

Title		
PCI EXPRESS X4 SLOT		
Size	Document Number	Rev
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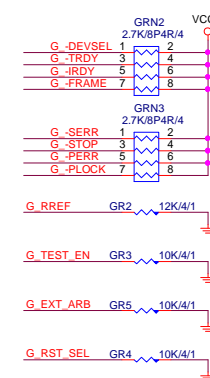
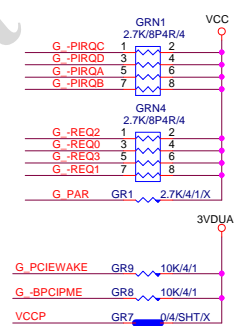


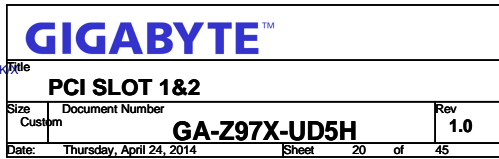
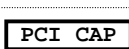
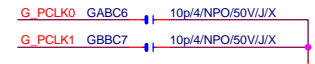
PCB layout note:
Close to chip



```
High: Enable PCI CLK 66MHz
Low: Disable PCI CLK 66MHz
```

High: PCICLK INPUT form CLK Gen
Low: PCICLK OUTPUT form IT8893 chip





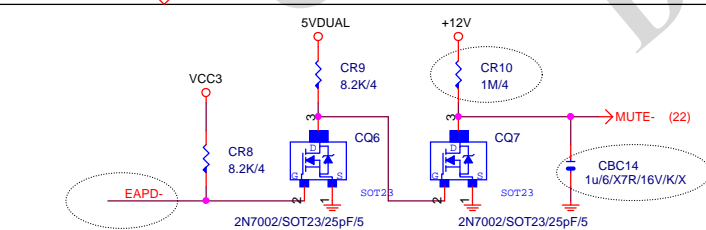
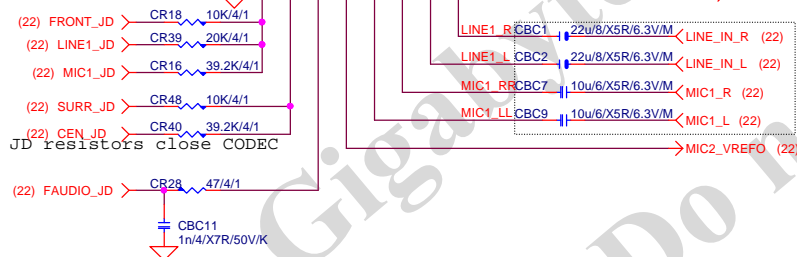
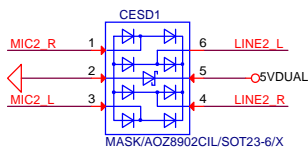
AZALIA CODEC

Thermal pad is DGND

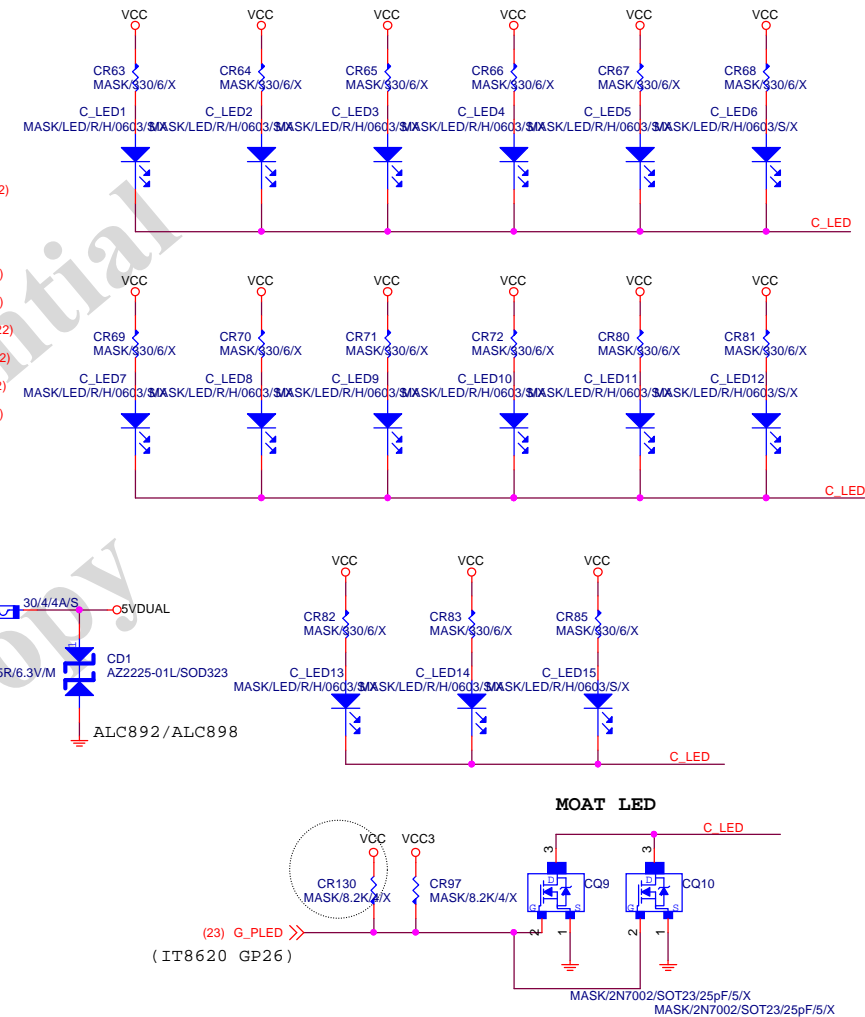
Digital Area

Analog Area

0/6/X For AGND/GND
moat under Codec
Body



UD5H不上金屬罩&LED



Gigabyte Technology

Title			HD AUDIO ALC887B-VD2/VT1708S/VT2021
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AZALIA JACK



CR23 2 2/6 → Audio jack → USB (各打2 VIA hole)

CR44 0/6/SHT/X → Under Audio jack (各打2 VIA hole)

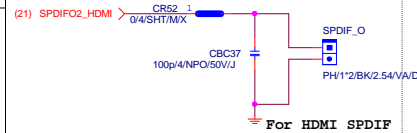
MOATR1 0/4/SHT/M/X
MOATC1 0.1u4/X7R/16V/K → Near F_AUDIO (各打2 VIA hole) **LINE-IN**

MOATR2 0/4/SHT/M/X
MOATC2 0.1u4/X7R/16V/K → Near Codec (各打2 VIA hole)

MOATR3 0/4/SHT/M/X
MOATC3 0.1u4/X7R/16V/K → Near R_AUDIO (各打2 VIA hole) **MIC-IN**

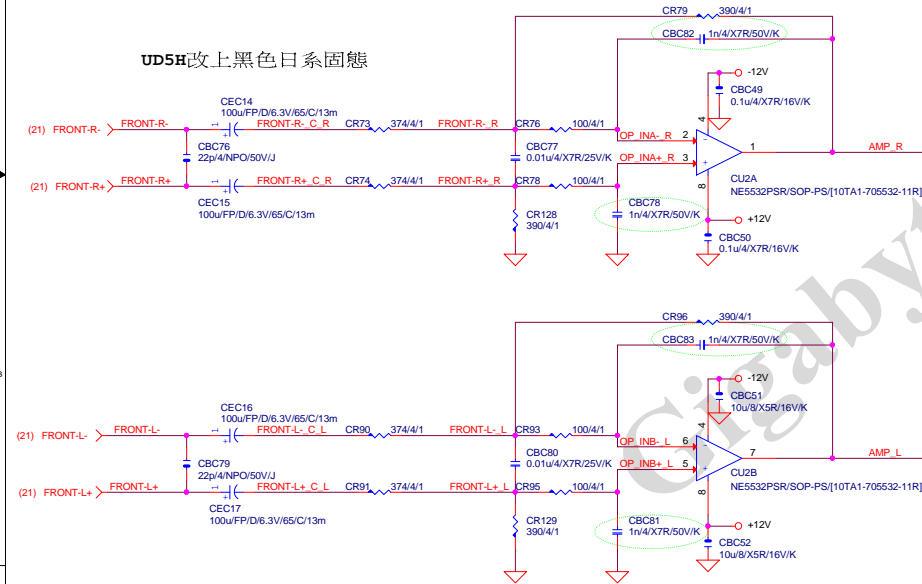
MOATR4 0/4/SHT/M/X
MOATC4 0.1u4/X7R/16V/K → Near AMP (各打2 VIA hole)

SPDIF_OUT

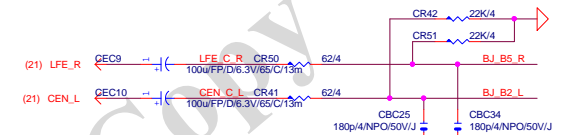
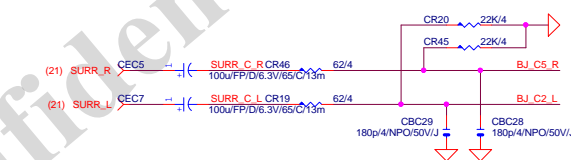
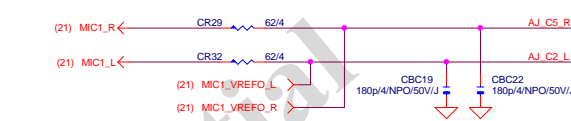
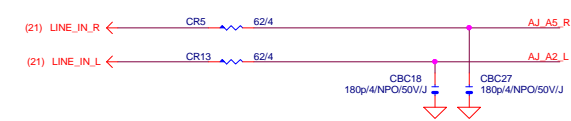
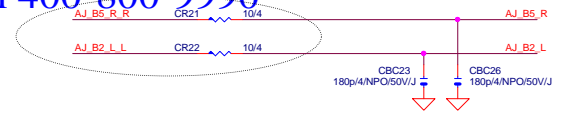
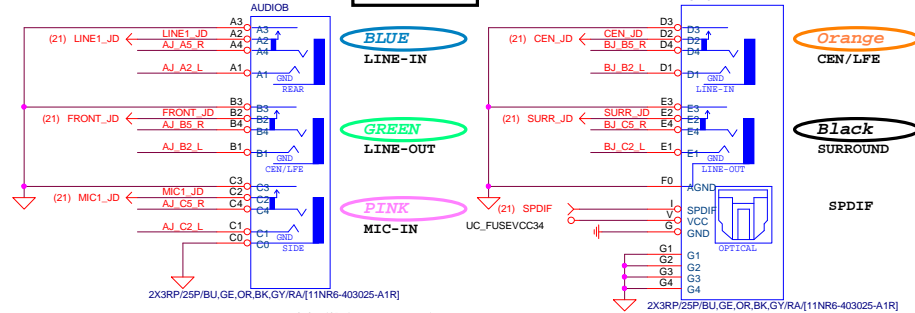


Differential to Single-End AMPLIFIED

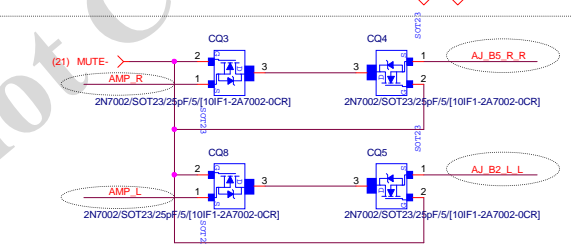
UD5H 改上黑色日系固态



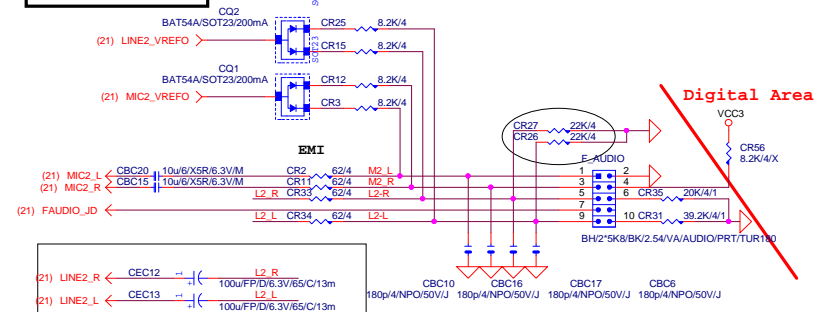
AZALIA JACK



Anti Pop

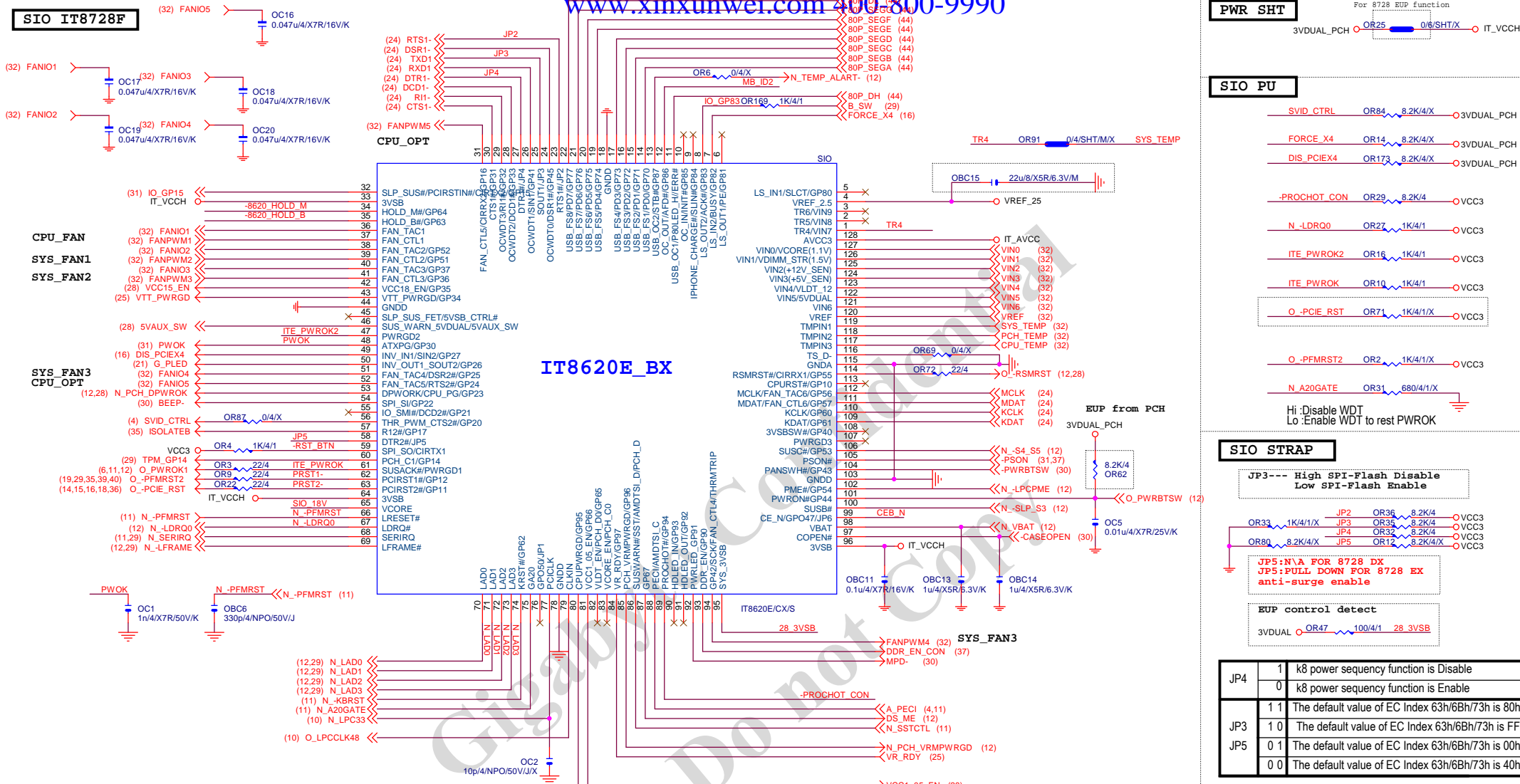


AZALIA FRONT PANE



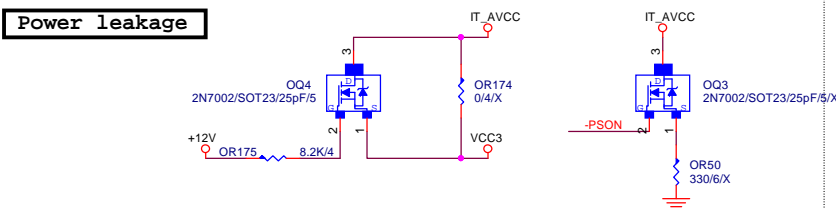
Gigabyte Technology

File			
AUDIO JACK			
Size	Document Number	Rev	
Custom	GA-Z97X-UD5H	1.0	
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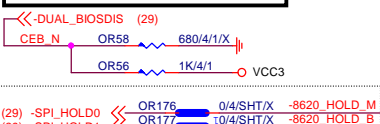


IT8620E GPIO問題匯整	
PIN 50	GP26--- 第一次接上POWER時會拉 LO
PIN 90/91	DEFAULT為HLED FUNCTION, GP93 BYPASS TO GP92 高溫時 會被拉Lo(ITE BUG)
PIN 108	GP40--- POWER ON 時會拉 LO
PIN 111/112	MOUSE 跟FAN6 FUNCTION 擇一使用,不然會互相干擾

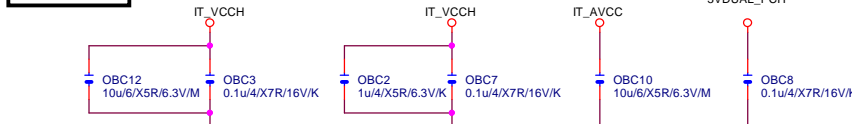
Power leakage



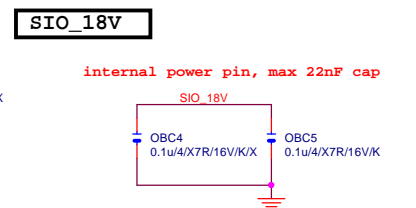
DUAL BIOS OPT STRAP



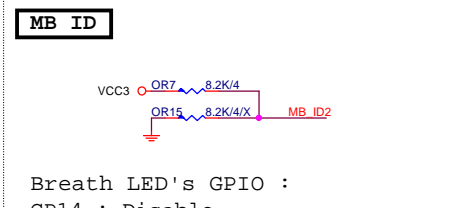
SIO CAP



SIO_18V



MB ID



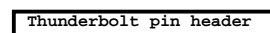
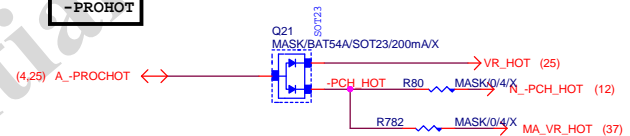
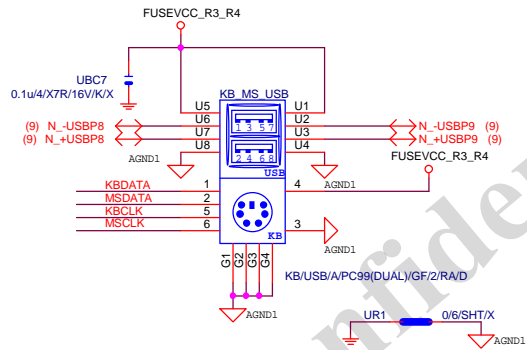
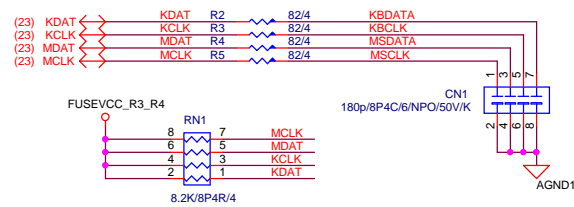
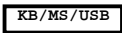
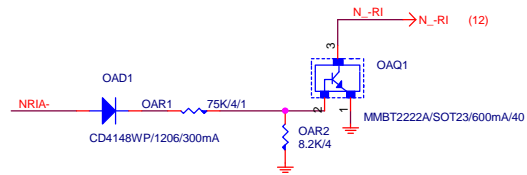
Breath LED's GPIO :

GP14 : Disable

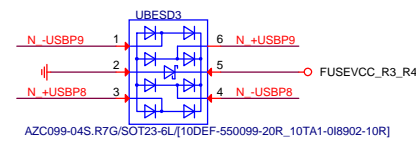
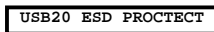
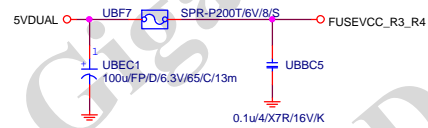
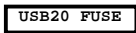
GP65 : Brightness

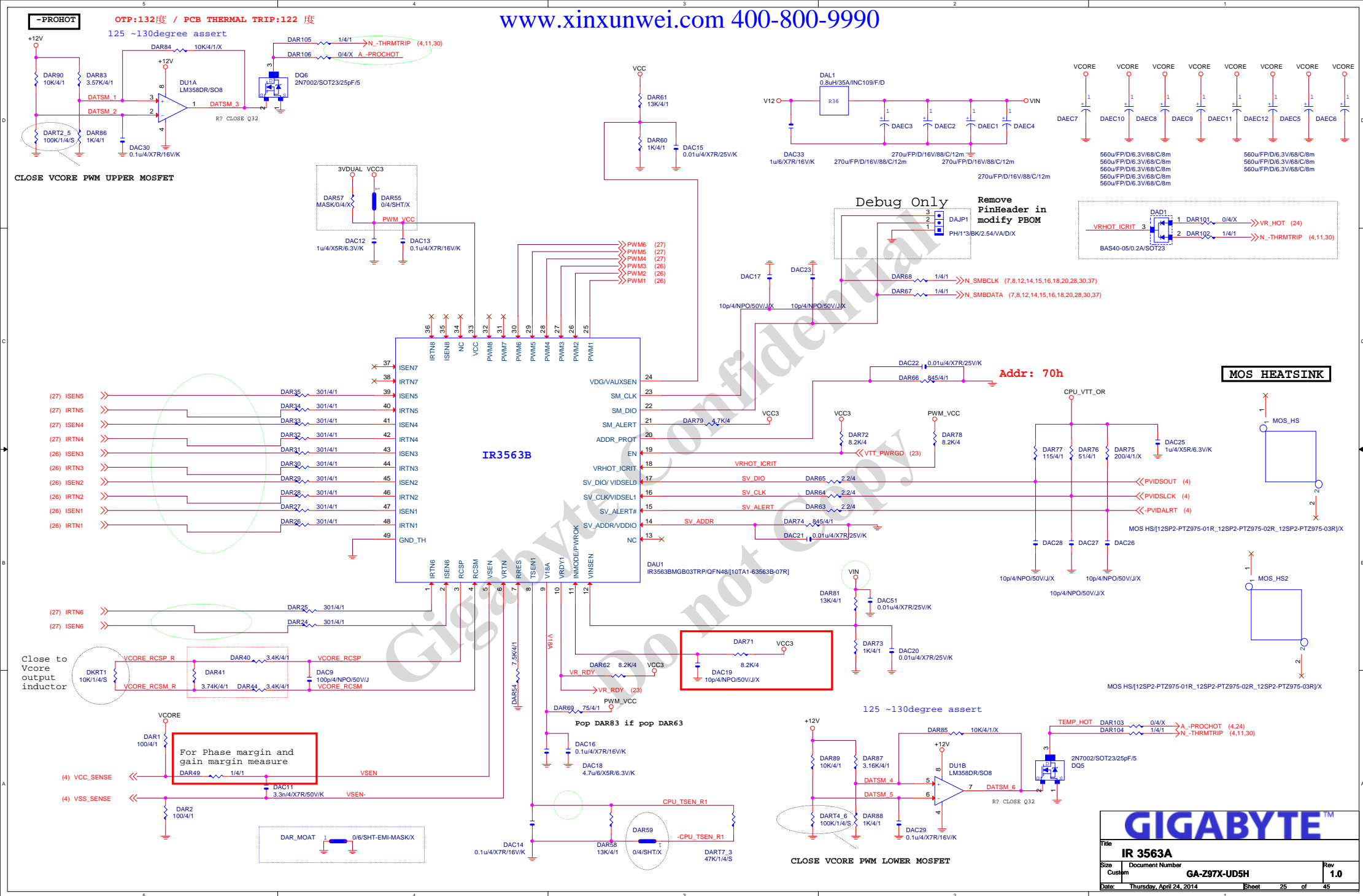
Gigabyte Technology

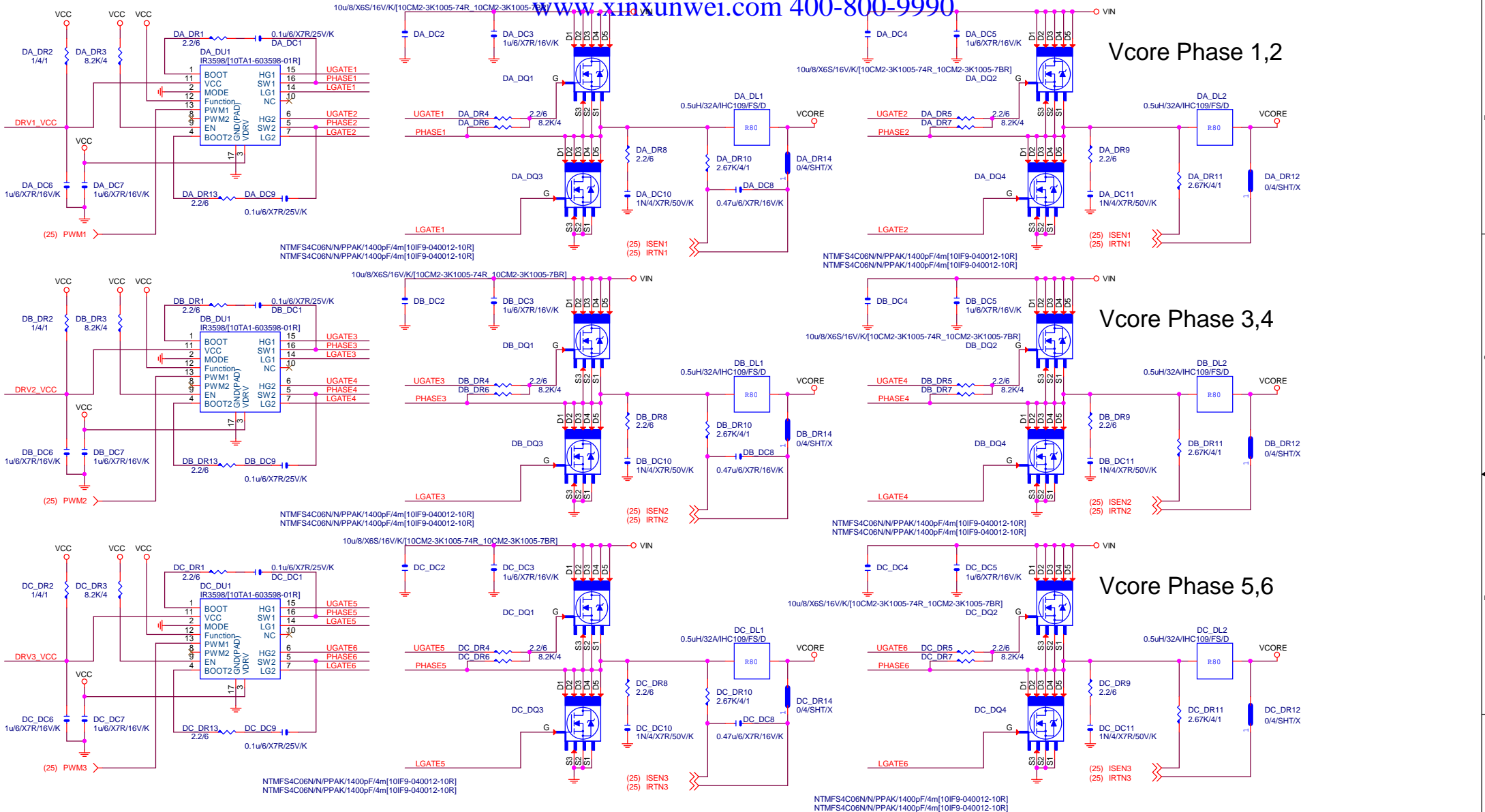
Title		ITE 8620CX LPC IO	
Size B	Document Number	GA-Z97X-UD5H	
Date:	Thursday, April 24, 2014	Sheet	23 of 45
Rev	1.0		



Removed







Vcore Phase 1,2

Vcore Phase 3,4

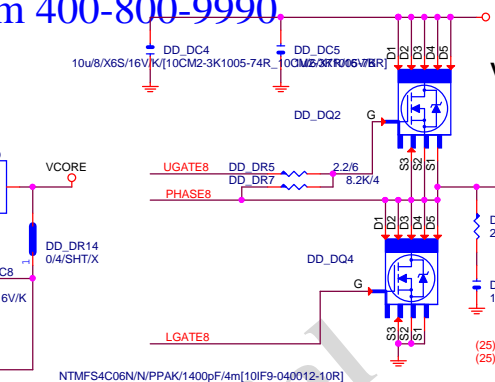
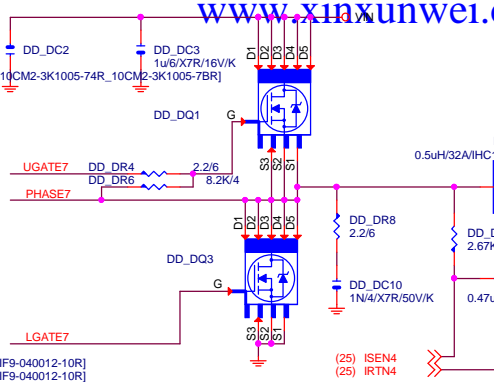
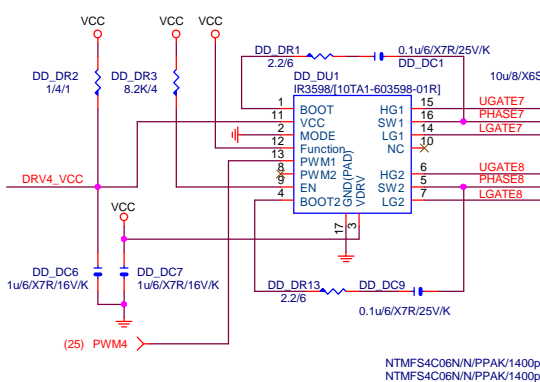
Vcore Phase 5,6

FUNCTION	MODE	PWM MODE	PHASE MODE
0	1	IR ATL	DUAL
1	1	IR ATL	Doubler
0	0	Tri-Sate	DUAL
1	0	Tri-Sate	Doubler
OPEN	0	Tri-Sate	Quad
OPEN	1	IR ATL	Quad

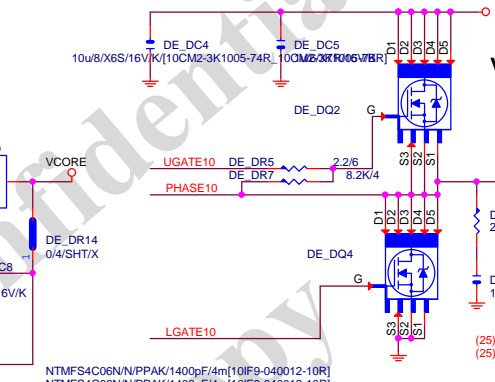
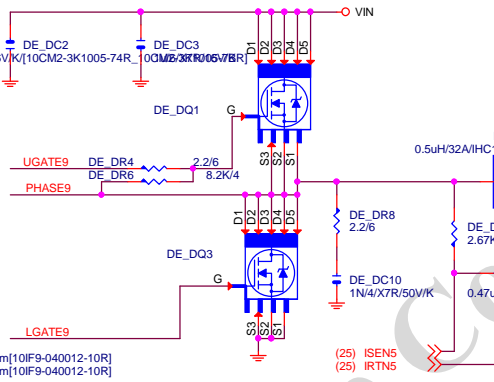
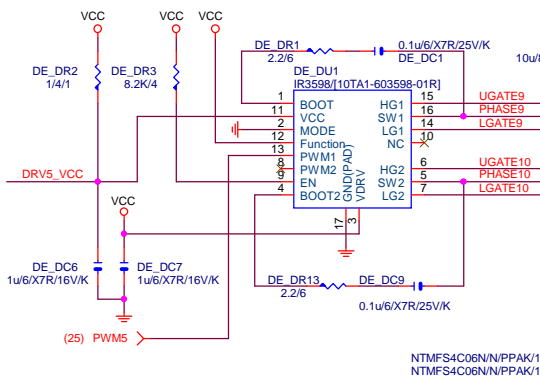
function = 0 --> Quad mode
function = 1 --> Doubled mode

In Quad mode , IC1 pin10 link to IC2 pin10
IC1 pin9 link to IC2 pin9 without PU

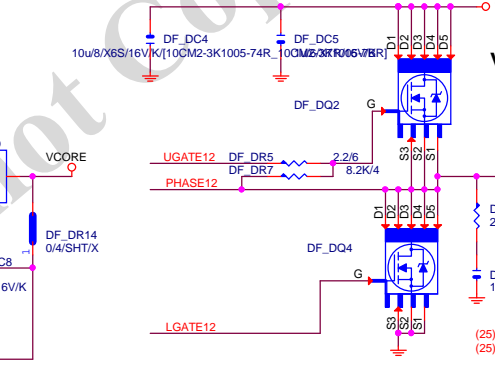
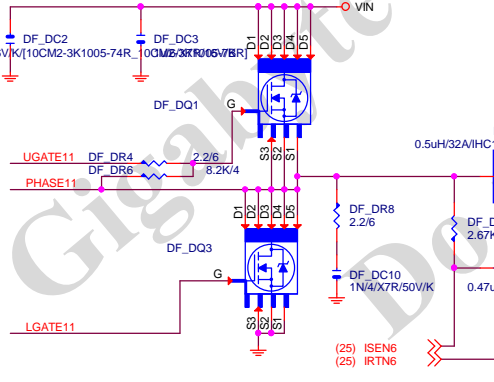
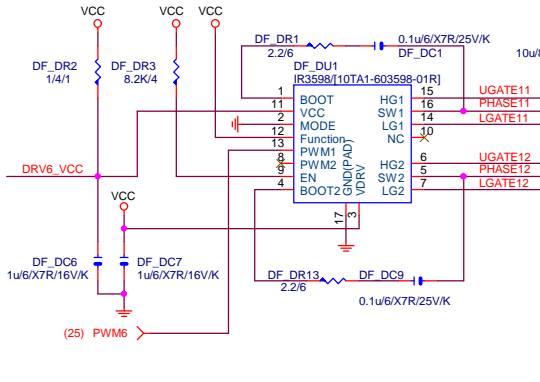
GIGABYTE TECHNOLOGY			
Title			
CPU CORE_IR3563B			
Size			
Document Number			
GA-Z97X-UD5H			
Rev			
1.0			
Date:			
Thursday, April 24, 2014			
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Vcore Phase 7,8



Vcore Phase 9,10



Vcore Phase 11,12

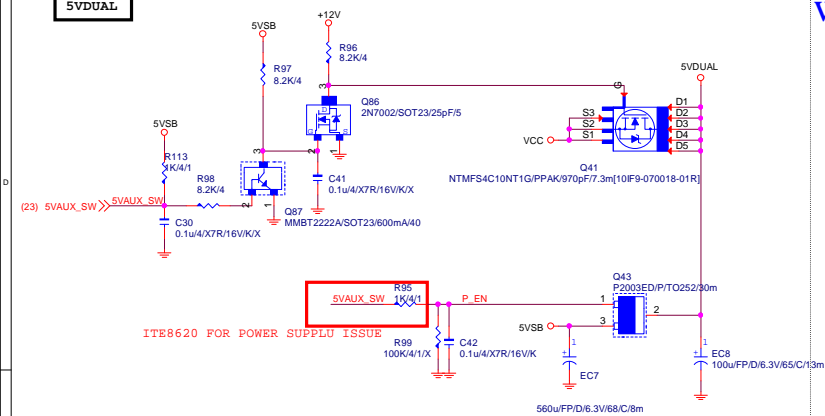
FUNCTION	MODE	PWM MODE	PHASE MODE
0	1	IR ATL	DUAL
1	1	IR ATL	Doubler
0	0	Tri-Sate	DUAL
1	0	Tri-Sate	Doubler
OPEN	0	Tri-Sate	Quad
OPEN	1	IR ATL	Quad

function = 0 --> Quad mode
function = 1 --> Doubled mode

In Quad mode , IC1 pin10 link to IC2 pin10
IC1 pin9 link to IC2 pin9 without PU

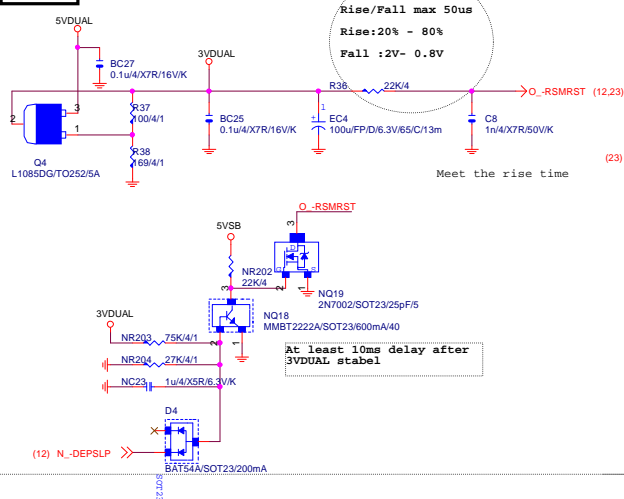
GIGABYTE TECHNOLOGY			
Title	CPU CORE_IR3563B		
Size	Document Number	Rev	
Custom	GA-Z97X-UD5H	1.0	
Date:	Thursday, April 24, 2014	Sheet	27 of 45

5VDUAL

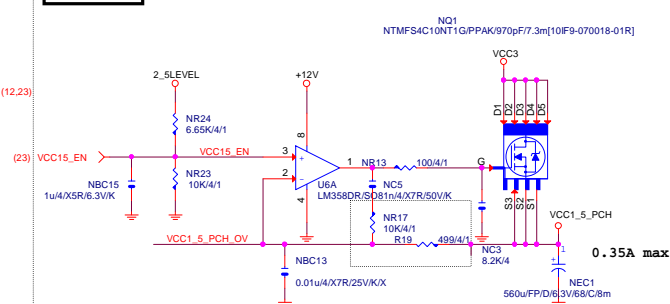


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5VDUAL

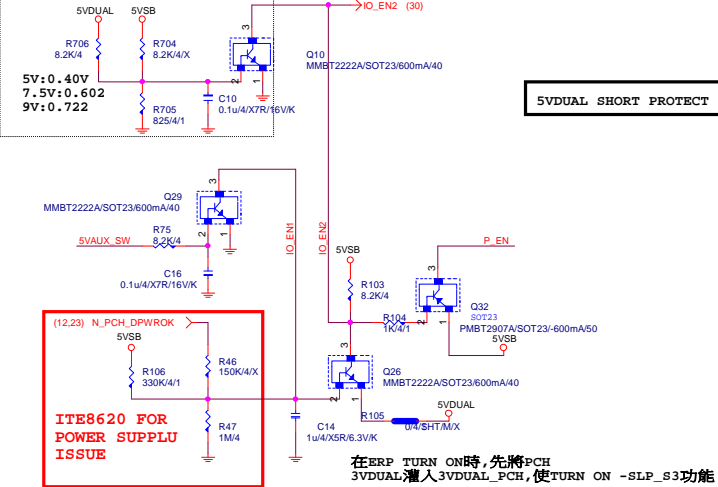


VCC1_5_PCH

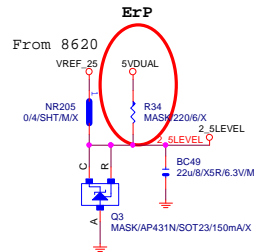


5VSB OVP:7.5V protection

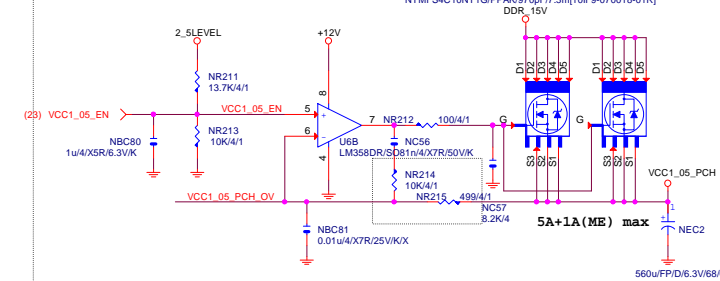
NOTE 82:改5VDUAL 6v保護



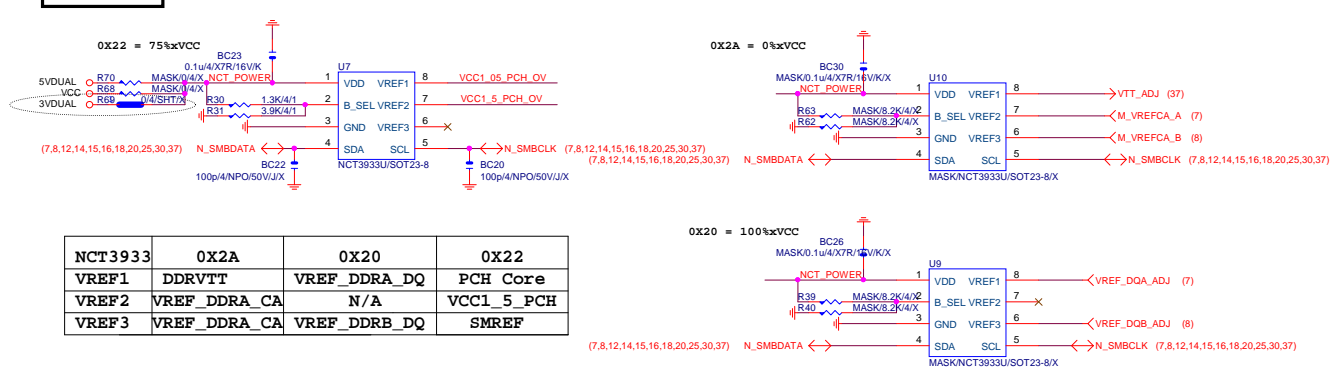
2_5LEVEL



VCC1_05_PCH



OVER VOLTAGE



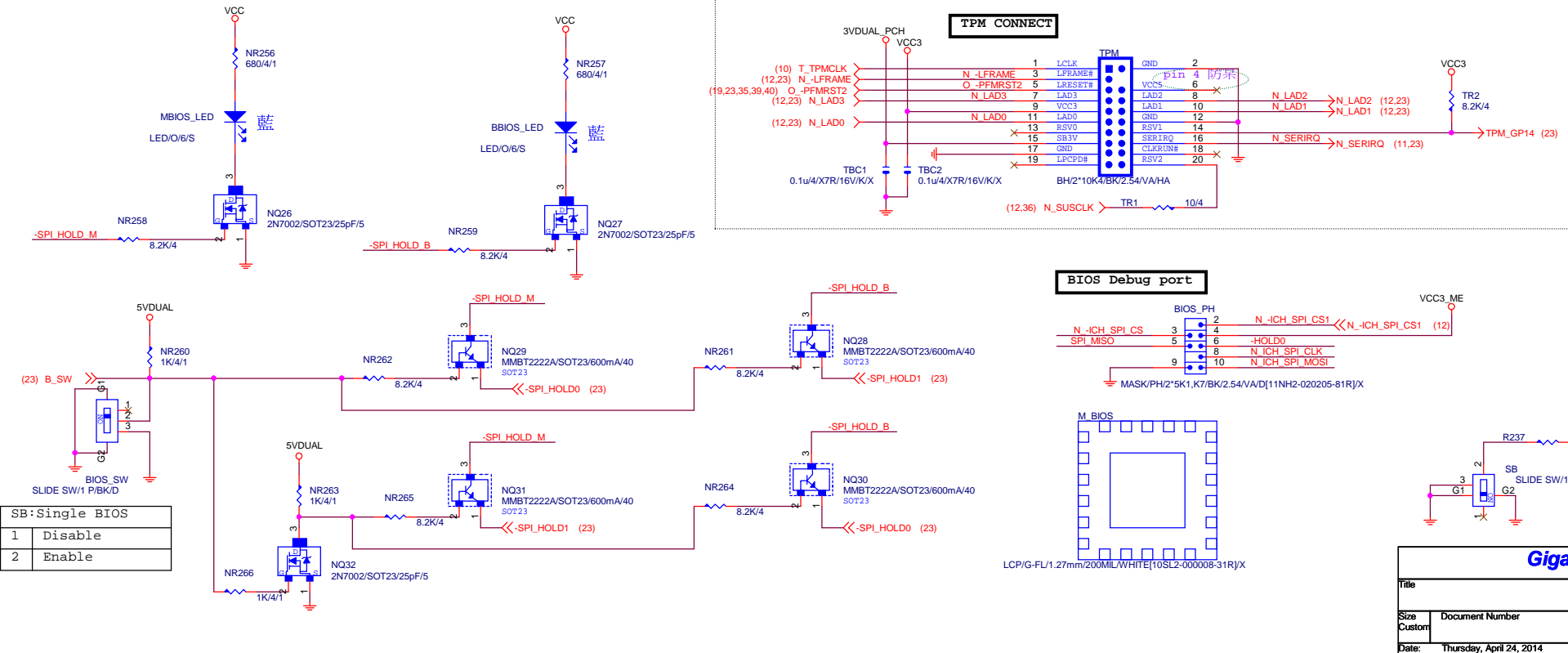
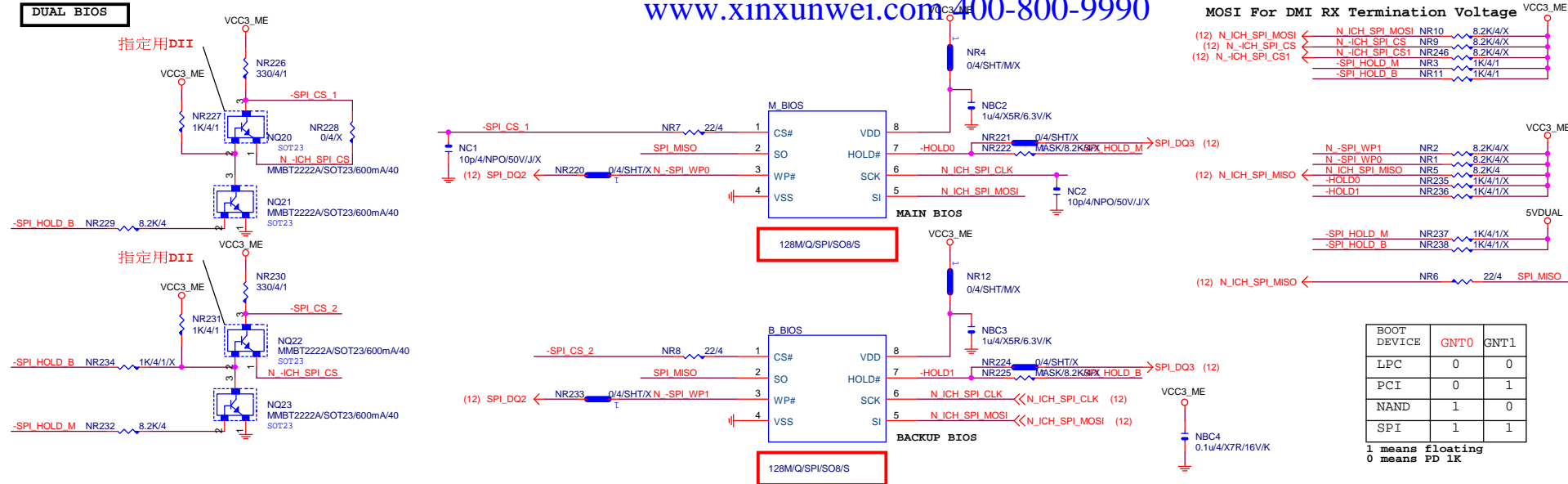
NCT3933	0X2A	0X20	0X22
VREF1	DDRVT	VREF_DDRA_DQ	PCH Core
VREF2	VREF_DDRA_CA	N/A	VCC1_5_PCH
VREF3	VREF_DDRA_CA	VREF_DDBR_DQ	SMREF

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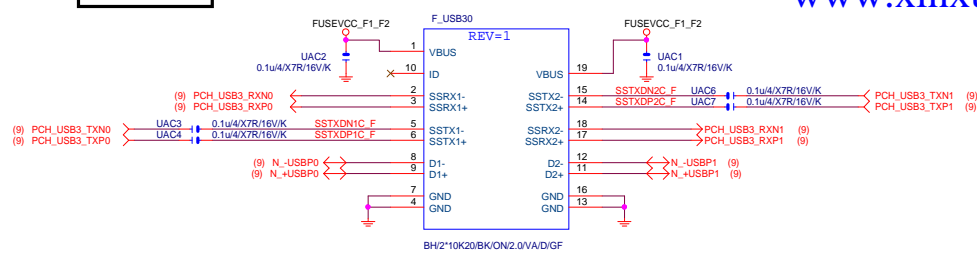
Title		
DISCRETE POWER		
Size	Document Number	Rev
Custom	GA-Z97X-UD5H	1.0
Date:	Thursday, April 24, 2014	Sheet 28 of 45

DUAL BIOS

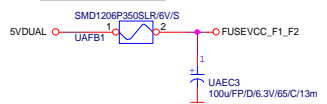
MOSI For DMI RX Termination Voltage



Front USB3.0

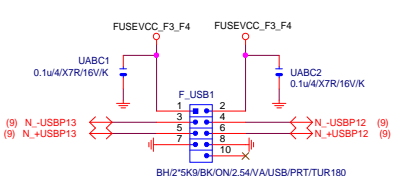


F_USB30 PWR

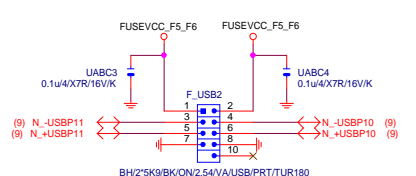


Close to connector

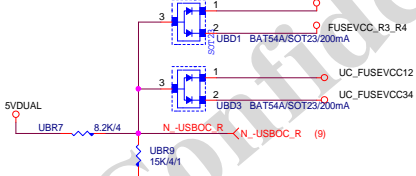
FRONT USB1



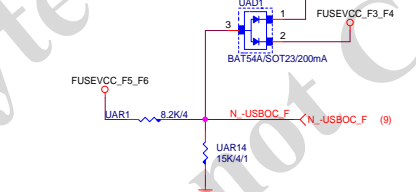
FRONT USB2



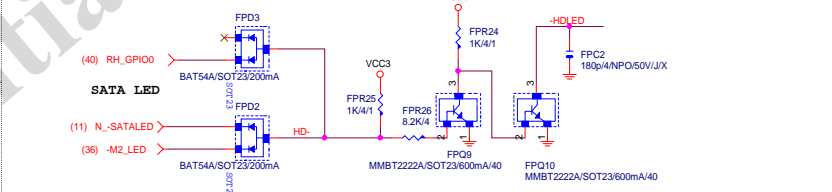
-USBOC_R



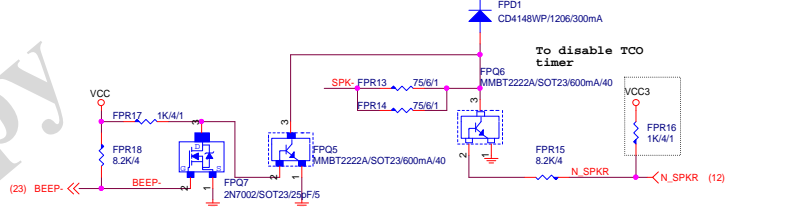
-USBOC_F



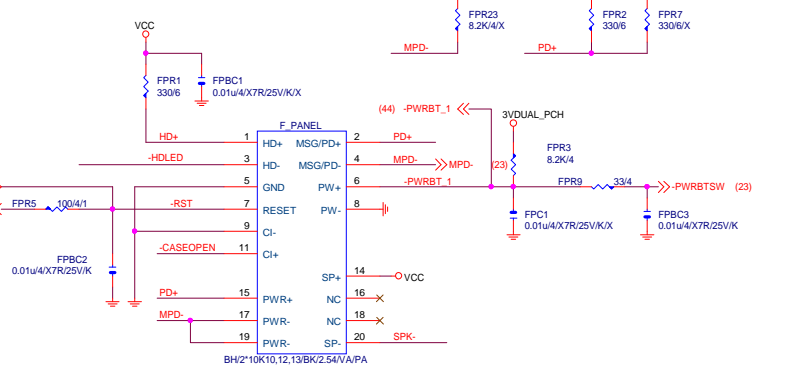
SATA LED SATALED# signal open-collector, pull-up (8.2 kΩ to 10 kΩ) to Vcc3_3



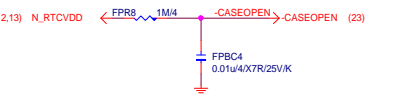
SPKR



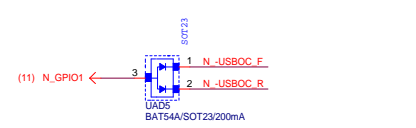
INTEL FRONT PANEL



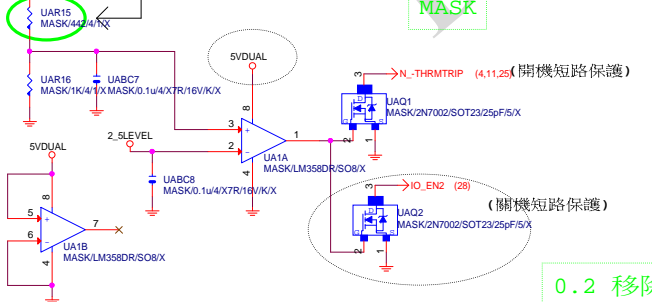
CASE OPEN



F_USB POWER PROTECT



USB2.0 Signal & power short protection

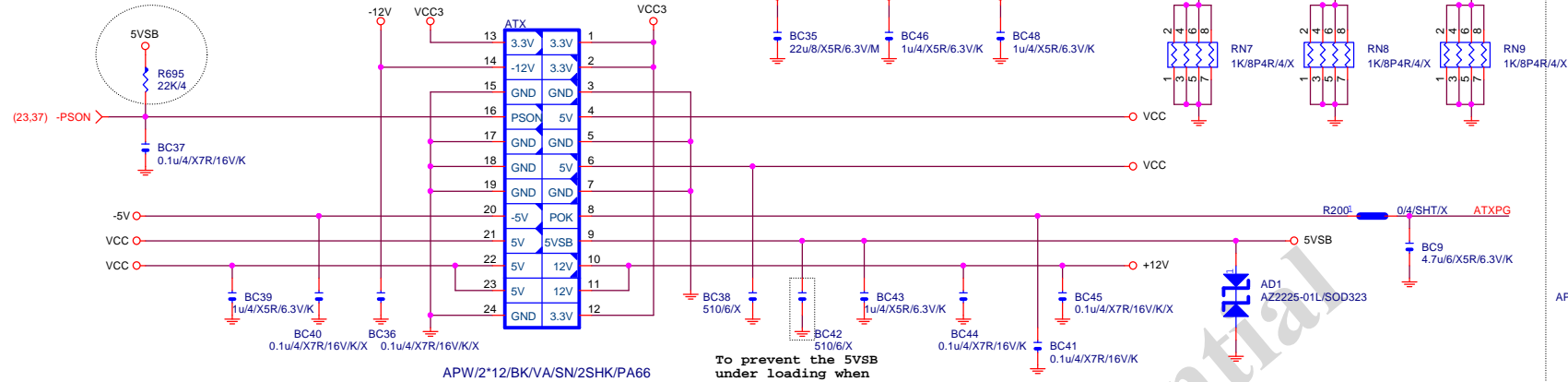
USB2.0 Signal > 4.85V
Enable --> 3VDUAL=3.6V

MASK

0.2 移除

ATXX24 POWER CONNECTOR

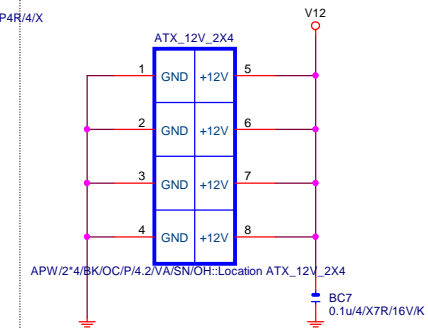
Patch some PSU no internal pull up resistor



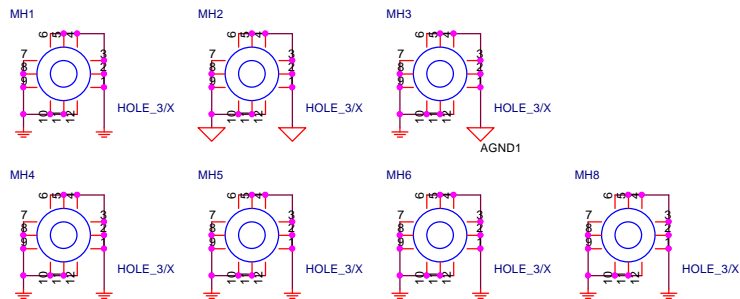
APW/2*12/BK/VA/SN/2SHK/PA66

To prevent the 5VSB under loading when boot

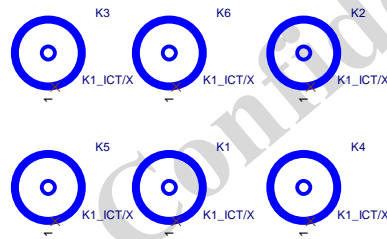
ATXX4 POWER CONNECTOR



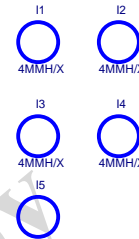
APW/2*4/BK/OC/P/4.2VA/SN/OH:Location ATX_12V_2X4



HOLE_4-RH-1



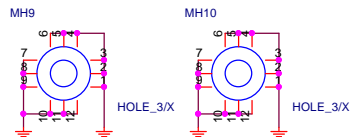
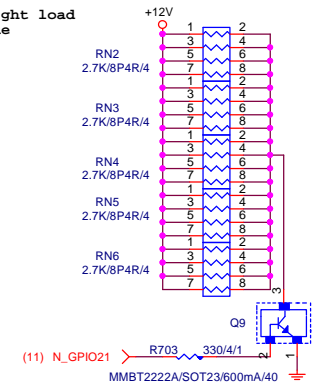
K1-ICT



4MMH

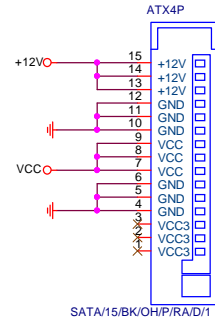
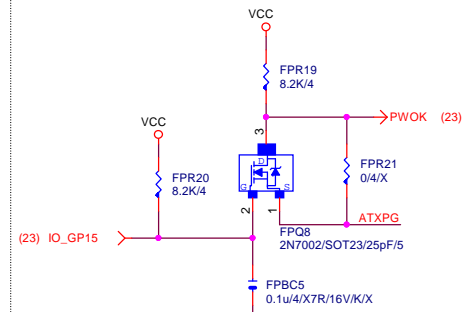
【技術通報R&D技術通報153】

To fix 12V light load abnormal issue



PWOK PATCH

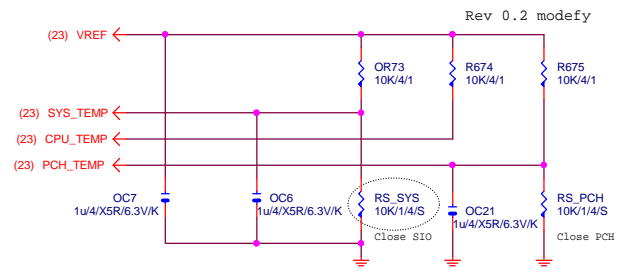
【技術通報R&D技術通報154】



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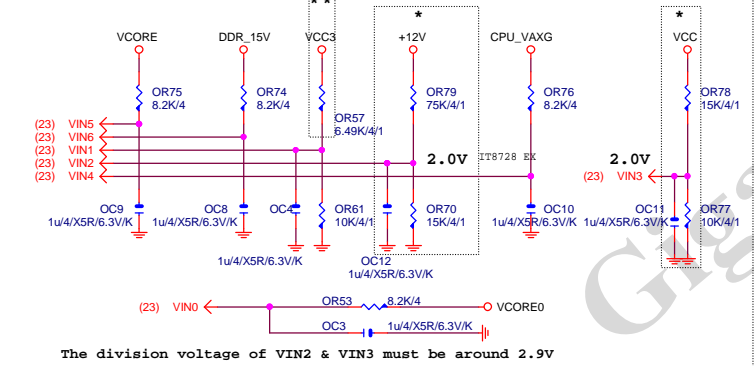
Title		
ATX POWER CONNECTOR		
Size	Document Number	Rev
Custom	GA-Z97X-UD5H	1.0
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TEMP H/W MONITOR



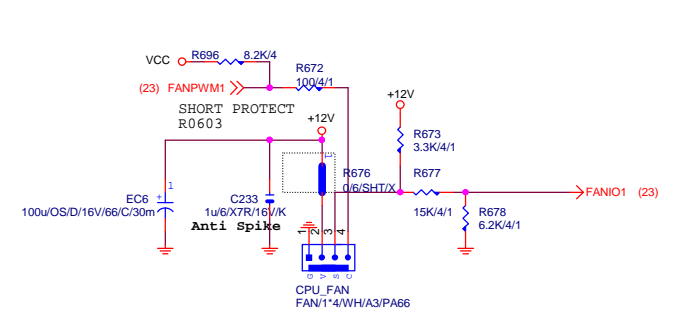
Thrmtrip#改用LM358做

VOLTAGE-- H/W MONITOR



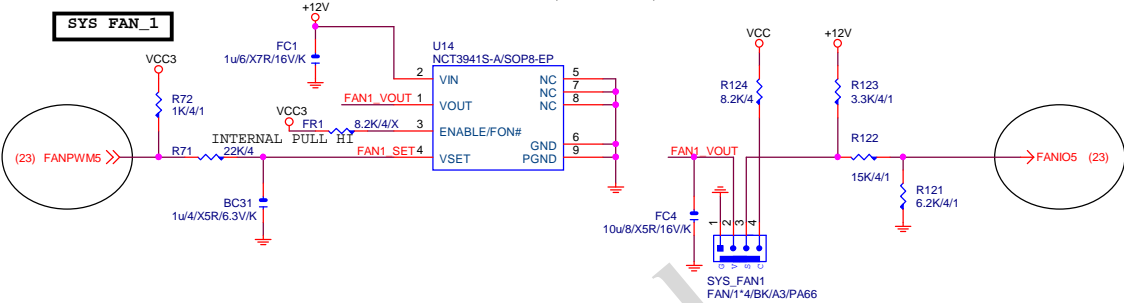
The division voltage of VIN2 & VIN3 must be around 2.9V

CPU SMART FAN

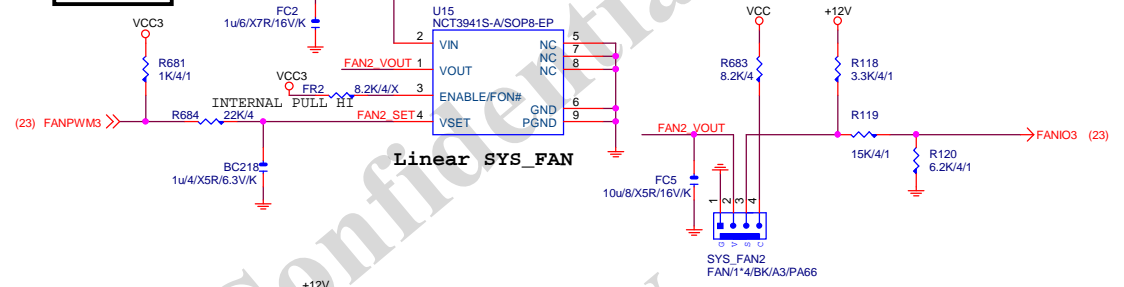


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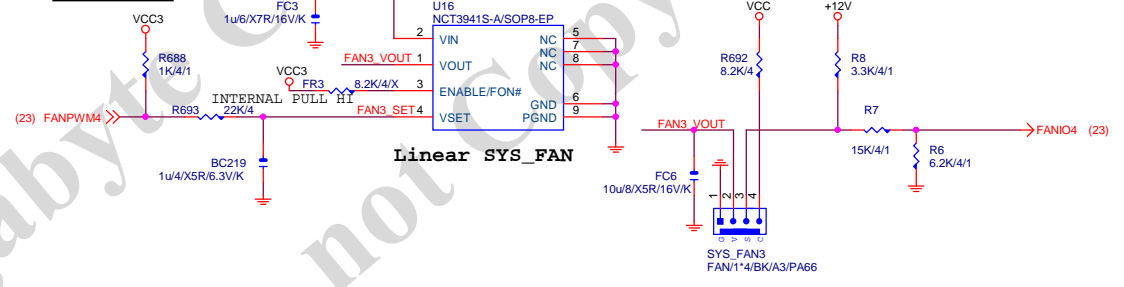
Linear SYS_FAN



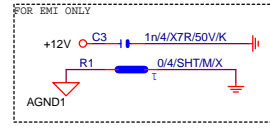
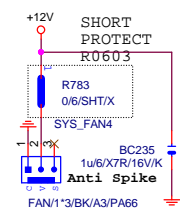
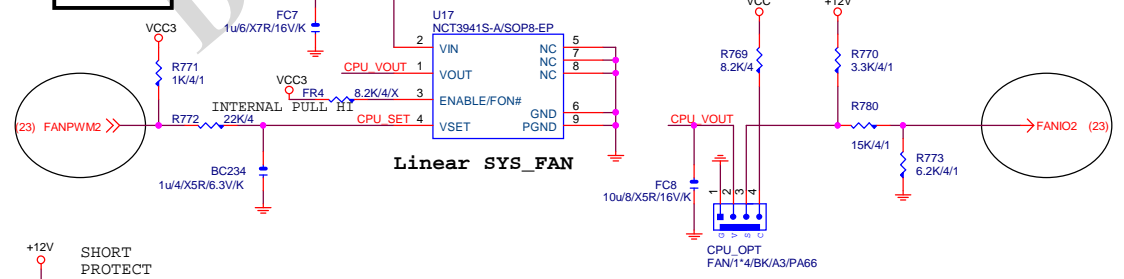
SYS_FAN_2



SYS_FAN_3



CPU_OPT



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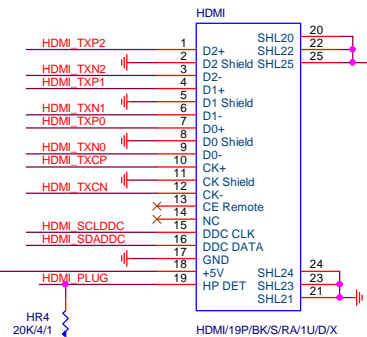
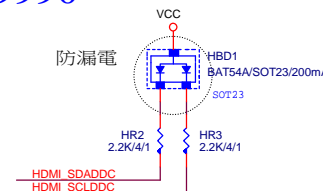
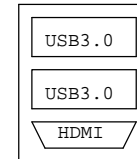
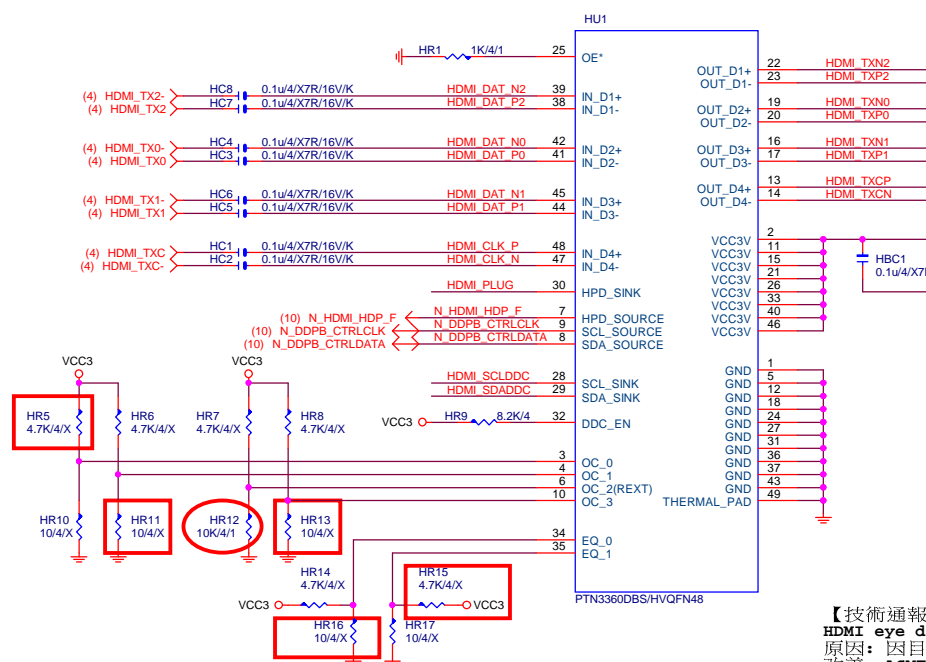
Title			HWM,KB/MS, FAN CTRL
Size	Document Number	Rev	
Custom	GA-Z97X-UD5H	1.0	
Date:	Thursday, April 24, 2014	Sheet	32 of 45

HDMI LEVEL SHIFT

HDMI:20/4/6/4/20

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Impedance=85 +- 17.5%

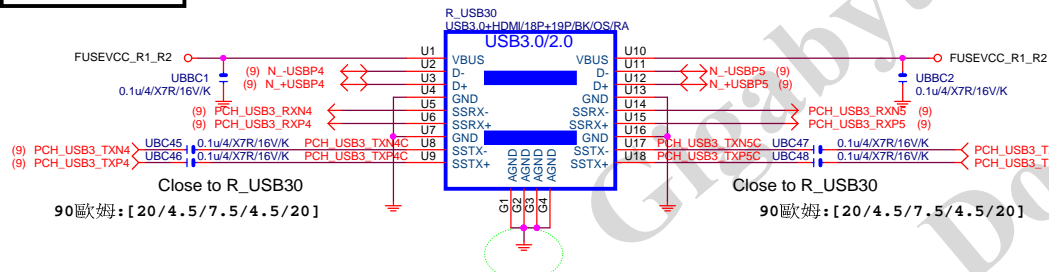


HDMI與R_USB共用一個料件

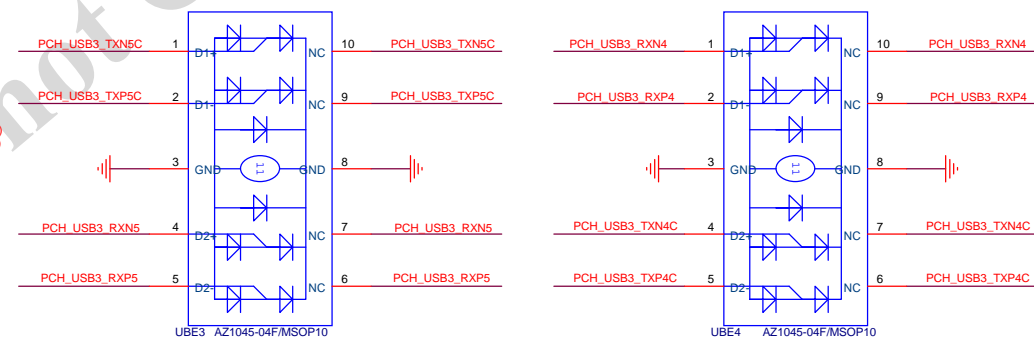
PTN3360:PIN 4/10/34/35 NC PIN,都不上值;只上HR12:10K
 ASM1442:紅色框要上,HR12:3.16K

【技術通報R&D技術通報150】
 HDMI eye diagram 1.4版(deep color)會fail
 原因: 因目前的HDMI訊號過長,造成RISING TIME過慢,而會壓到eye diagram
 改善: ASMEDIA ASM1442 : 3.16K(PIN6 PULL DOWN電阻) 10ohm(PIN4 PULL DOWN電阻)

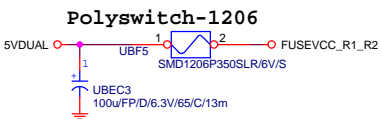
USB30_20 CONNECT



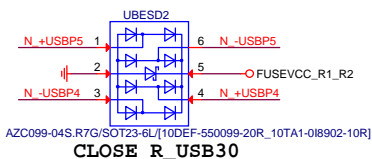
USB30 ESD PROTECT



USB30 PWR

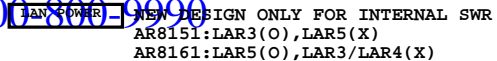


USB20 ESD PROTECT

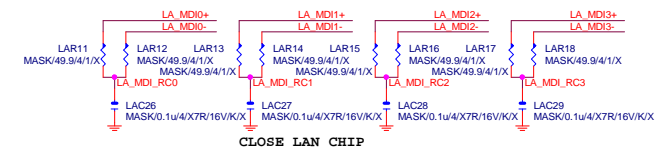
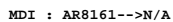


USB3.0 1Port - 1Fuse (3.5A)

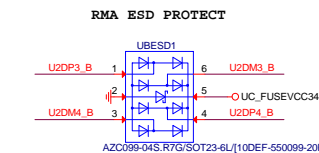
GIGABYTE™			
Title			
HDMI			
Size	Document Number	Rev	
Custom	GA-Z97X-UD5H	1.0	
Date:	Thursday, April 24, 2014	Sheet	34 of 45



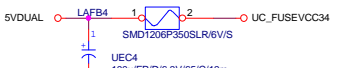
	AR8151	AR8161
AVDD33	N/A	3.3V
VDD33	3.3V	3.3V
AVDDH	2.7V	2.7V
AVDDL/DVDDL	1.1V	1.1V
VDDCT	1.7V	



USB_LAN CONNECTOR



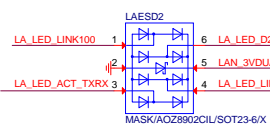
USB X3 POWER



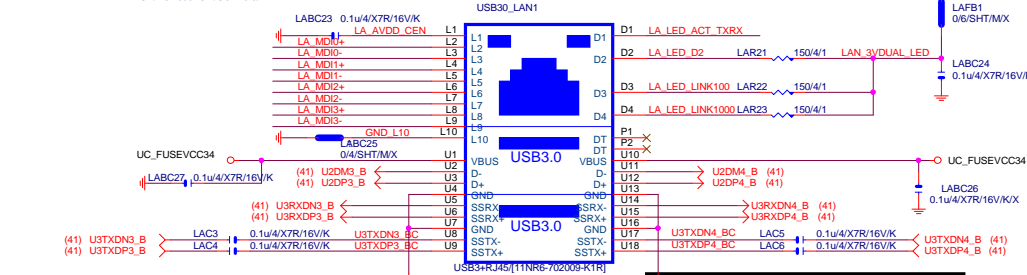
Close to connector

EMI SHORT PAD

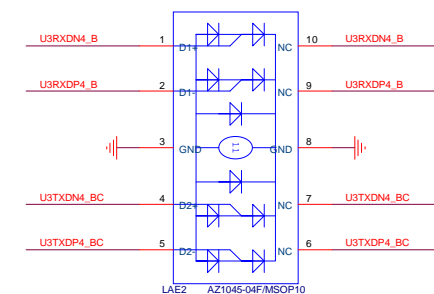
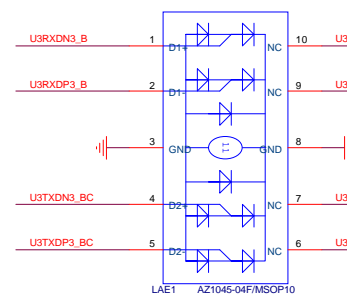
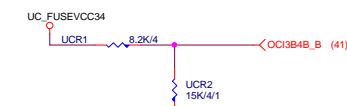
PS:視EMI需求



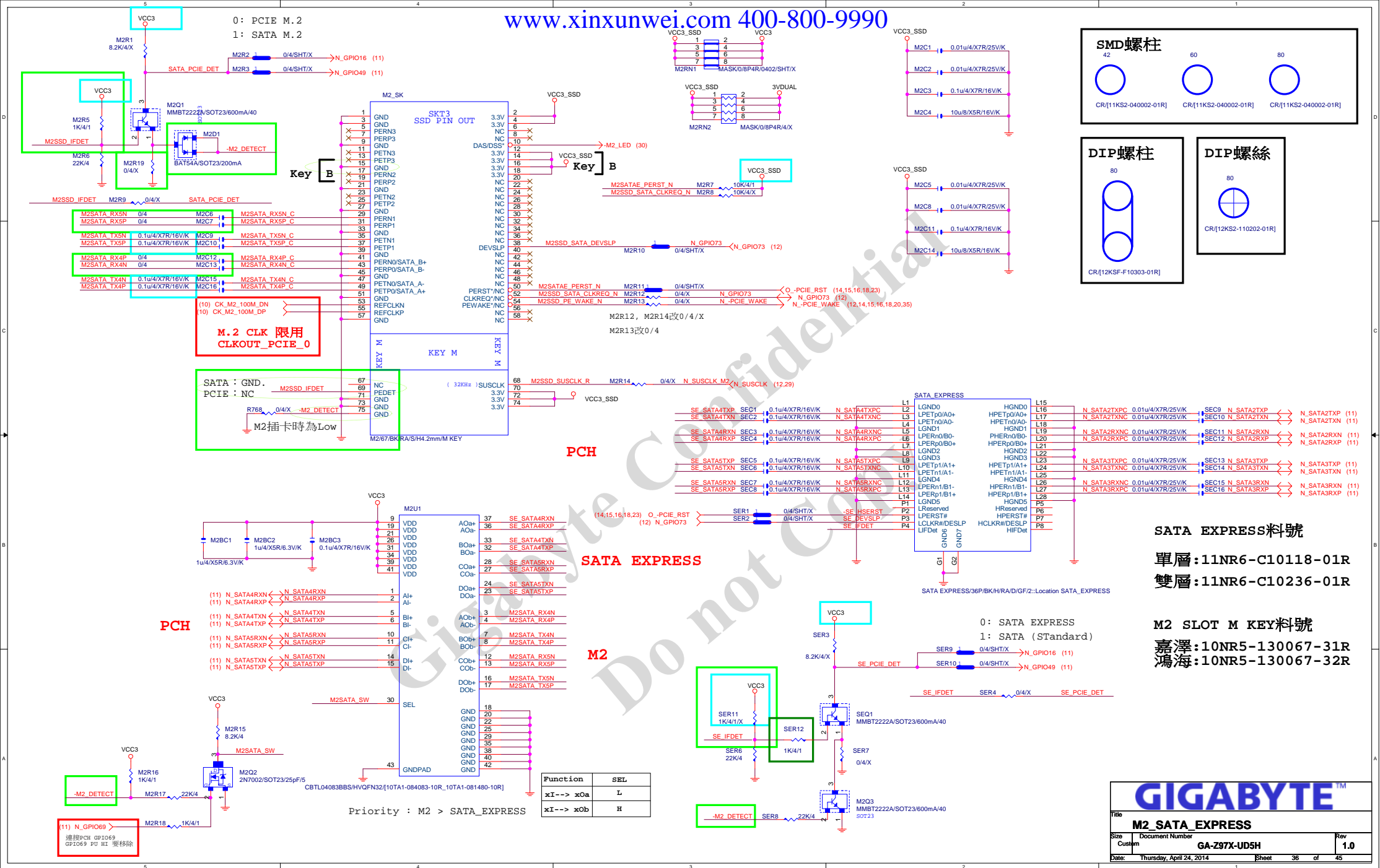
LA_MDI-->100歐姆:[20/4/8/4/20]



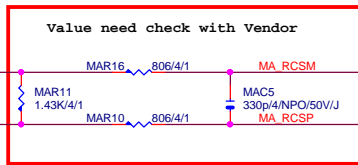
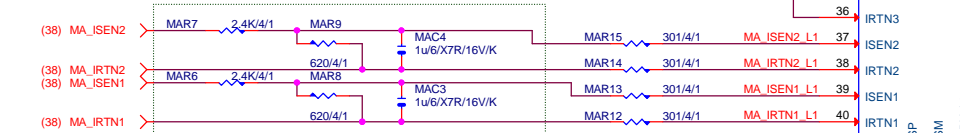
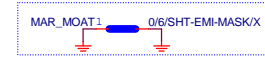
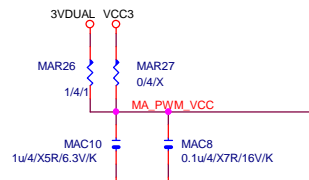
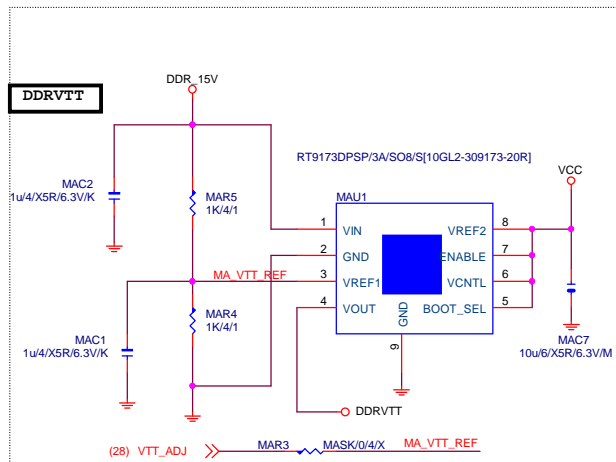
注意:USB PORT(目前:暫代6,7PORT)
USB-->90歐姆:[15/4.5/7.5/4.5/15]



Title			
ARTHEROS AR8151/AR8161			
Size Custom	Document Number	GA-Z97X-UD5H	Rev 1.0
Date:	Thursday, April 24, 2014	Sheet 35 of 45	

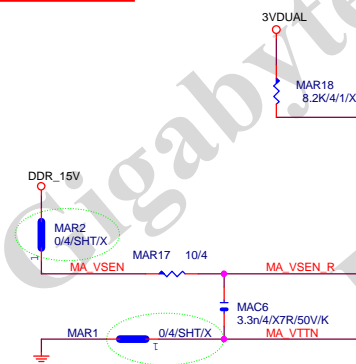
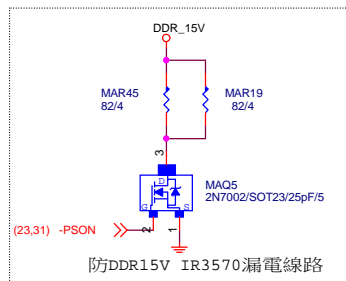
**GIGABYTE™**

Title			
M2_SATA_EXPRESS			
Size	Document Number	Rev	
Custom	GA-Z97X-UD5H	1.0	
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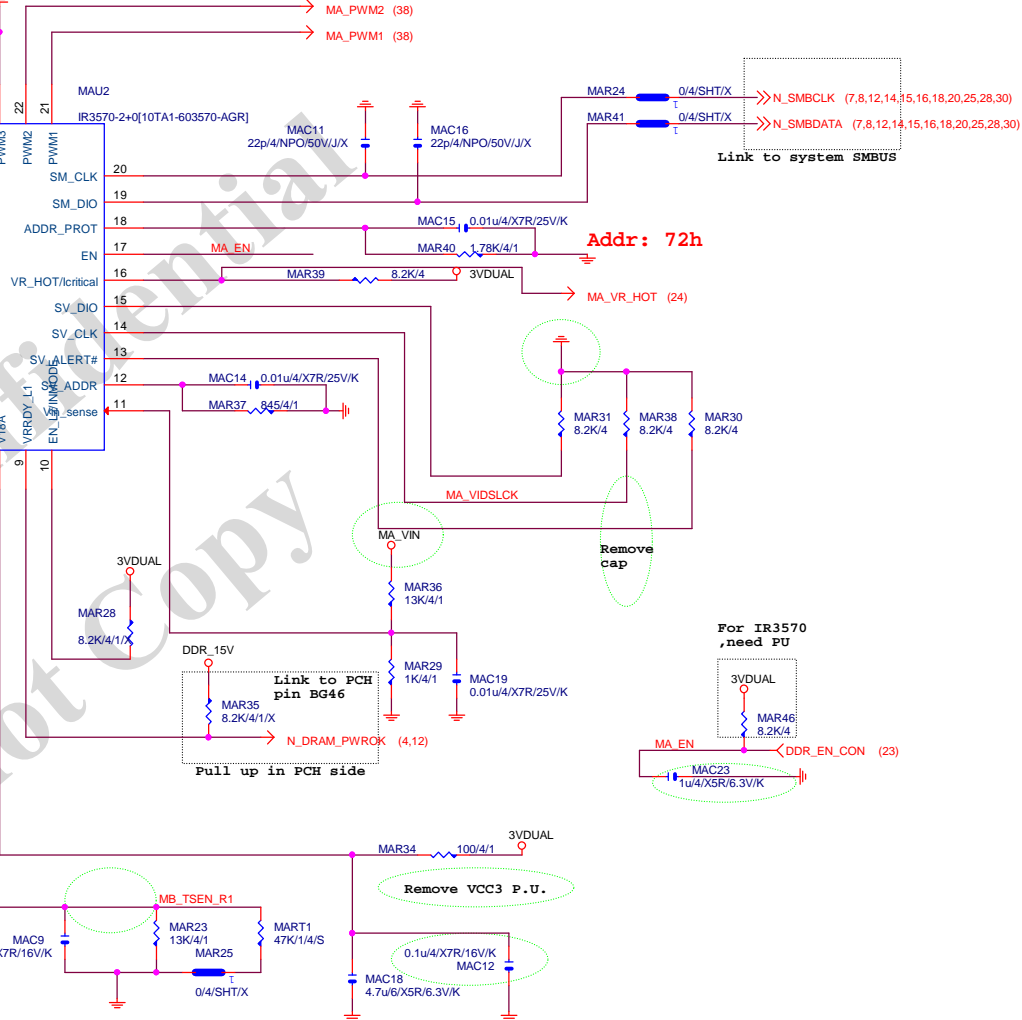


Close to DDR output inductor

should be routed as differential pair, 7mil width, 8mil spacing



IR3570



Link to system SMBUS

Addr: 72h

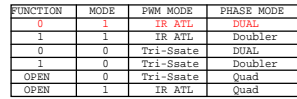
Remove cap

For IR3570, need PU

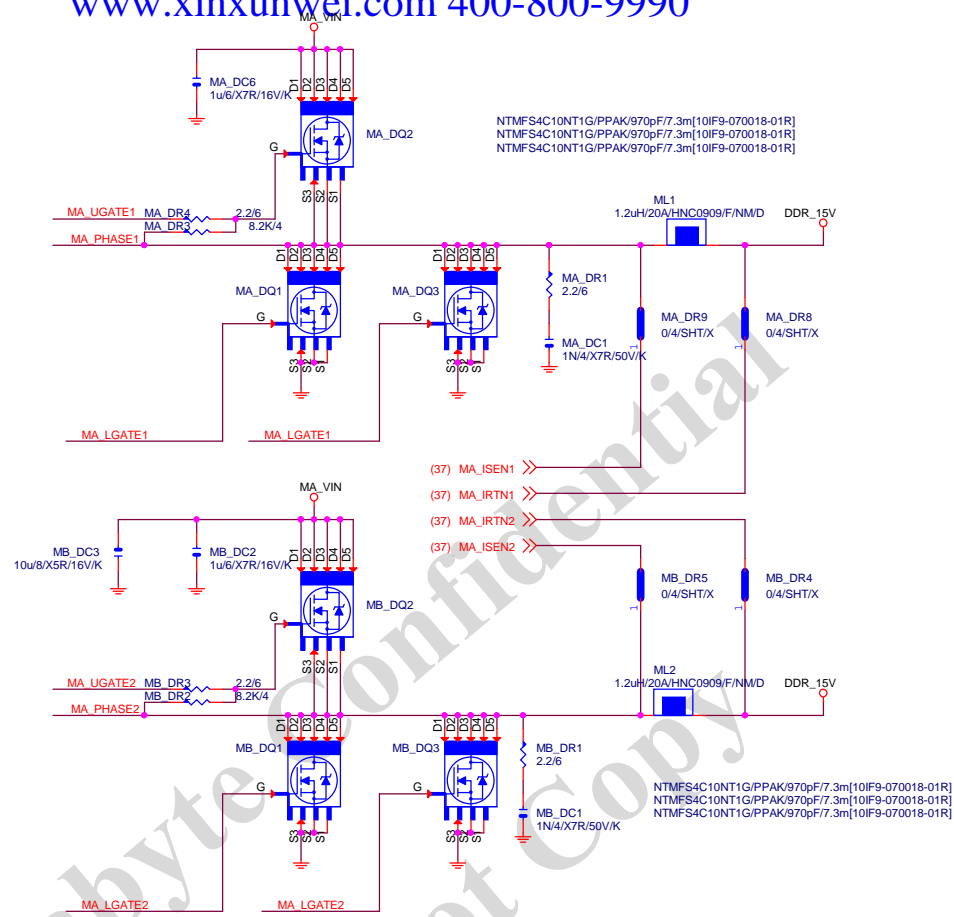
Link to PCH pin BG46

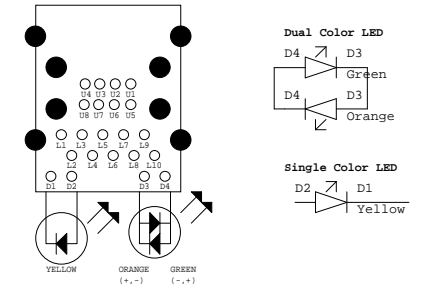
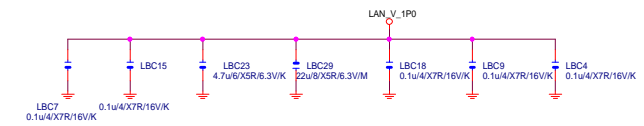
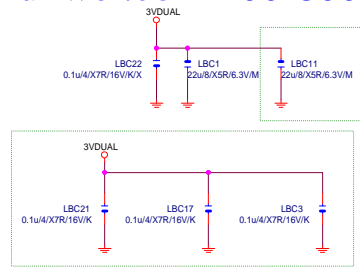
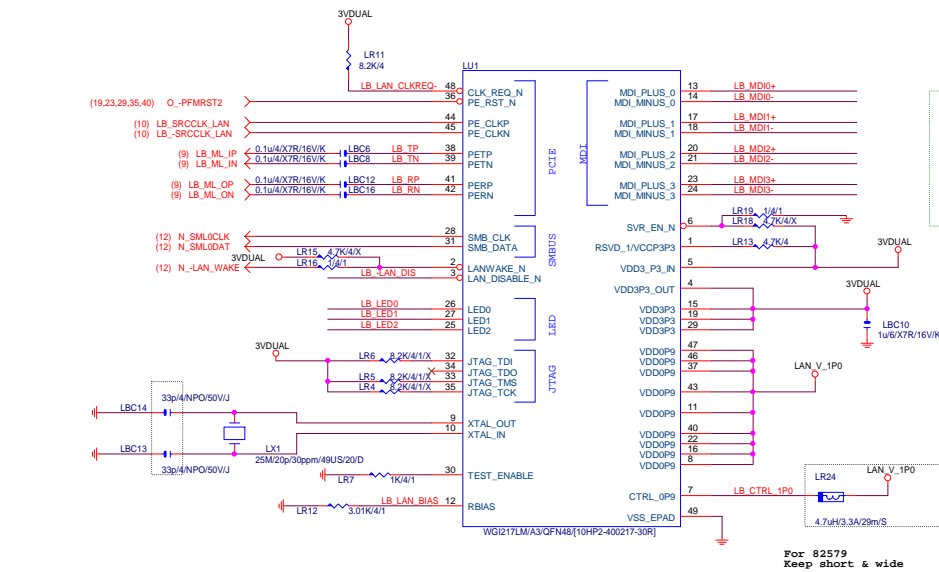
Remove VCC3 P.U.

GIGABYTE™			
Title			
DDR POWER IR3570			
Size	Document Number	Rev	
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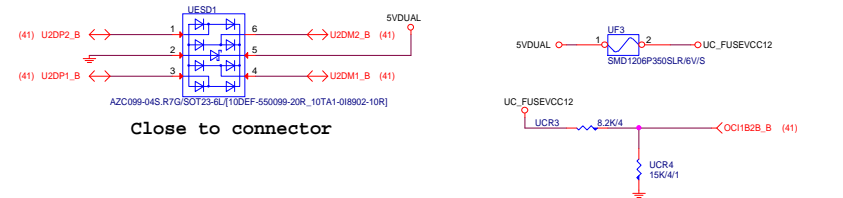
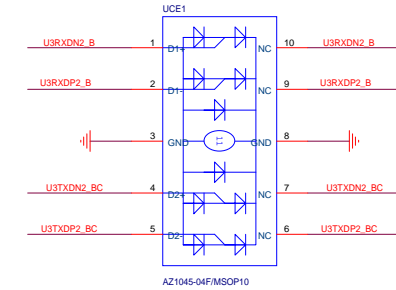
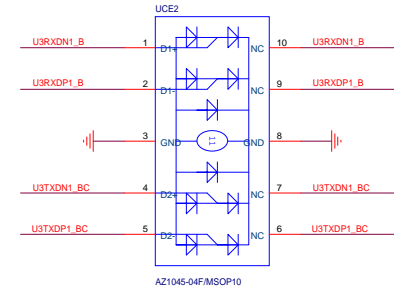
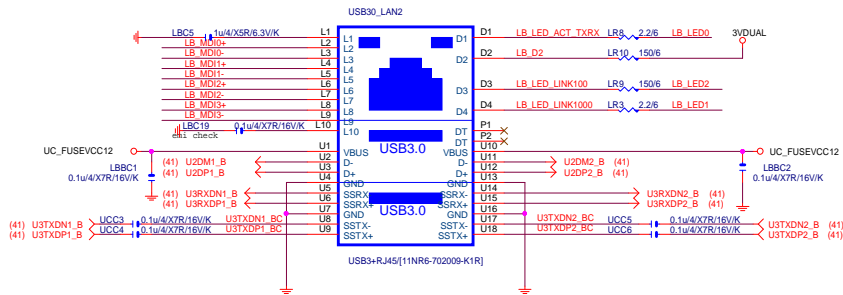
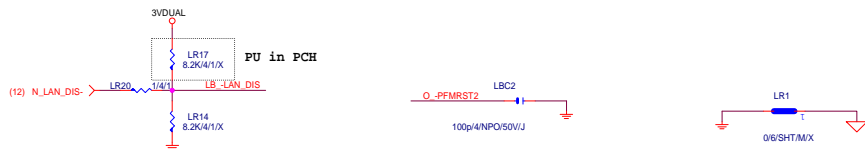
The schematic diagram illustrates the power supply circuit for the MA3000 module. It features a 5VDUAL input connected to a network of capacitors and an inductor. A 'Close Choke' section contains a 0.1uF/4X7R/16V/K capacitor (MAC13) and a 1.2uH/20A/HNC0909/F/NM/D inductor. A 'Close MOS' section includes a 1uF/6X7R/16V/K capacitor (MAC21) and a 1uF/6X7R/16V/K capacitor (MAC22). The circuit also includes a 1uF/6X7R/16V/K capacitor (MAC17) and a 1uF/6X7R/16V/K capacitor (MAC21). The output of the circuit is connected to the MA3000 module, which is powered by a 12V input and a 5VDUAL input. The module's internal components, including the MA3000 module and the MA3000 module, are shown in a detailed view.



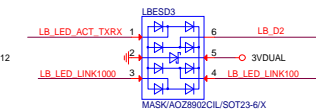
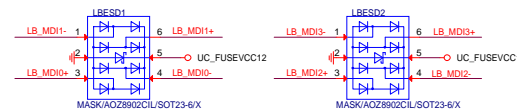


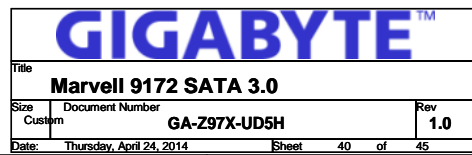
1Gb	Orange
100Mb	Green
10Mb	OFF

Access	Blinking
Link	Yellow



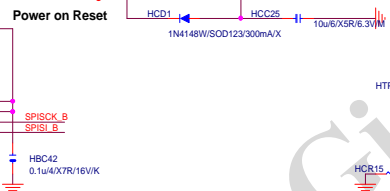
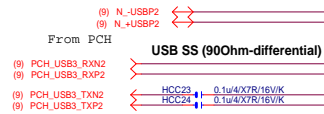
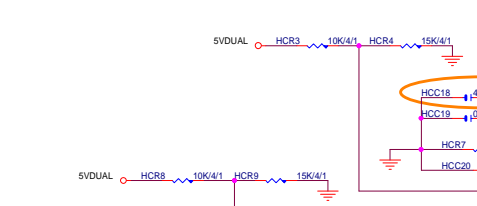
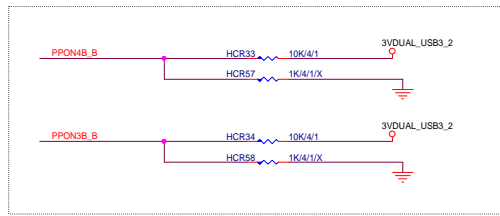
RMA ESD PROTECT



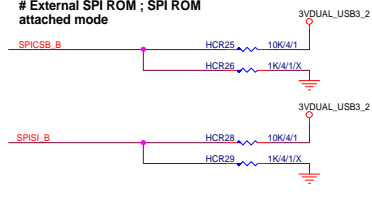


Number of Ports ; 4Ports mode

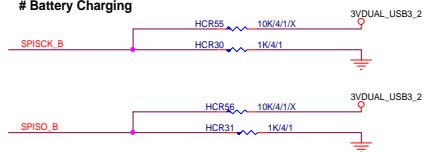
PPON3B / PPON4B : H / H (4 port)
 PPON3B / PPON4B : L / L (2 port)



External SPI ROM ; SPI ROM attached mode



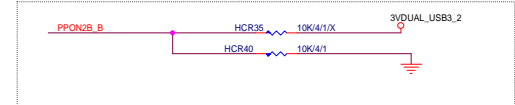
Battery Charging



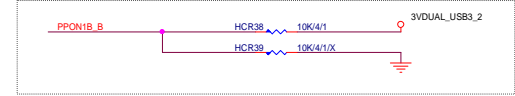
Put close to U1
 Do check with crystal vendor
 if the value of C31, C32 and
 R31 are all appropriate.

Put close to U1
 Short and broad connection to GND
 Don't split R32 into multiple
 resistors.

#5 VBUS Power Control ; Individual mode



PPON1B Pin Function ; Port1 PPONB mode

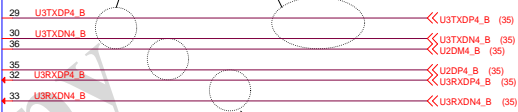


uPD720210

USB HS (90Ohm-differential)

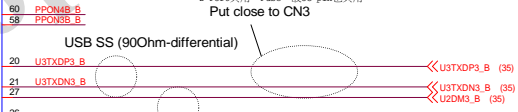
USB SS (90Ohm-differential)

Put close to CN4



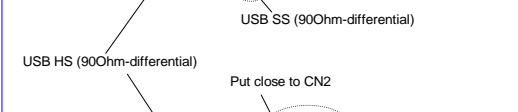
USB SS (90Ohm-differential)

Put close to CN3



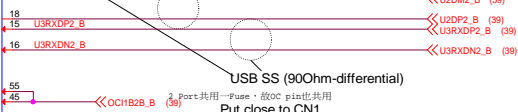
USB SS (90Ohm-differential)

Put close to CN2



USB HS (90Ohm-differential)

Put close to CN1



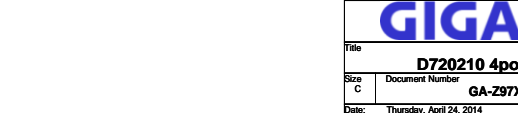
USB SS (90Ohm-differential)

Put close to CN1



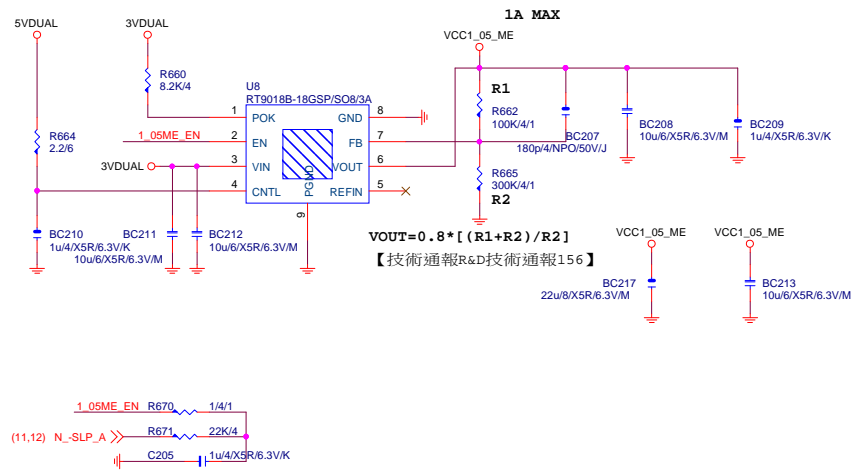
USB HS (90Ohm-differential)

Put close to CN1

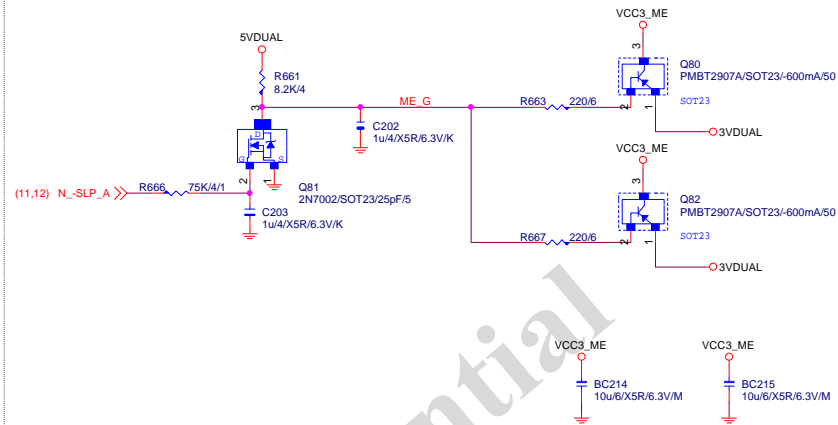


GIGABYTE™			
Title			
D720210 4port Hub B			
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VCC1_05_ME



VCC3_ME1



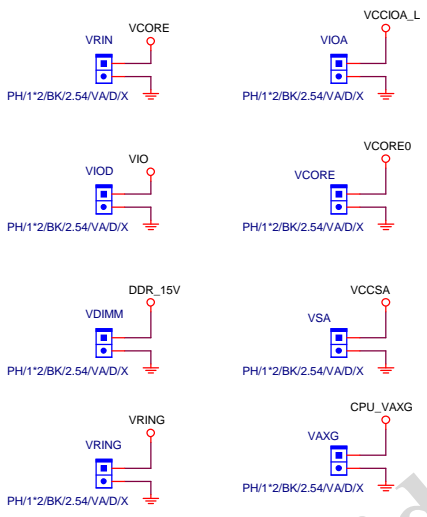
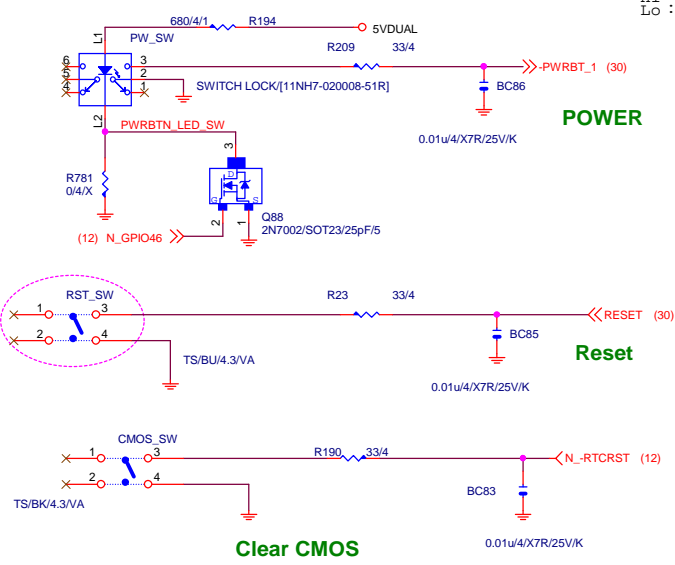
Gigabyte Confidential

Do not Copy

GIGABYTE™

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Hi : Button's LED ON
Lo : Button's LED OFF



80 PORT

